LMP91200 Configurable AFE for Low-Power Chemical-Sensing Applications

1 Features

- Active Guarding
- Key Specifications

  Unless otherwise noted, typical values at T_A = 25°C, V_S = (VDD-GND) = 3.3 V
  - pH Buffer Input Bias Current (0 < V_{INP} < 3.3 V)
    - Maximum at 25°C: ±125 fA
    - Maximum at 85°C: ±445 fA
  - pH Buffer Input Bias Current (–500 mV < V_{INP}– V_{CM} < 500 mV), V_S = (VDD – GND) = 0 V
    - Maximum at 25°C: ±600 fA
    - Maximum at 85°C: ±6.5 pA
  - pH Buffer Input Offset Voltage: ±200 µV
  - pH Buffer Input Offset Voltage Drift: ±2.5 µV/°C
  - Supply Current: 50 µA
  - Supply Voltage: 1.8 V to 5.5 V
  - Operating Temperature Range: –40°C to 125°C
  - Package: 16-Pin TSSOP

2 Applications

- pH Sensor Platforms

3 Description

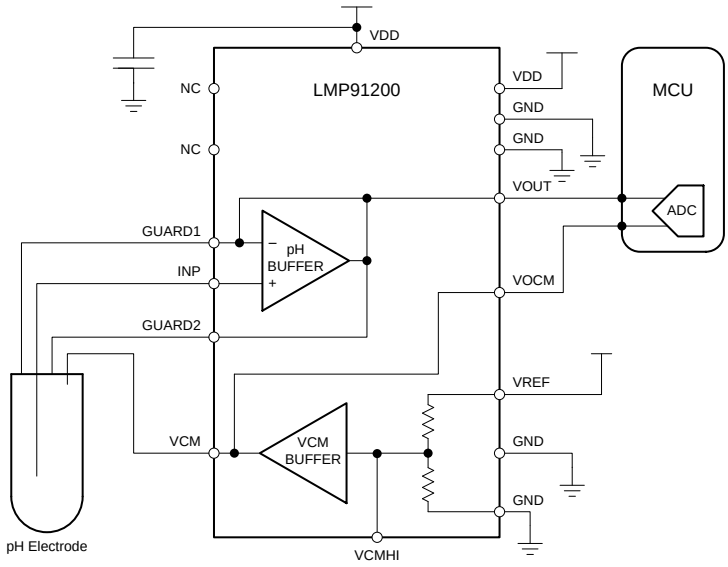
The LMP91200 device is a sensor AFE for use in low-power, analytical-sensing applications. The LMP91200 is designed for 2-electrode sensors. This device provides all of the functionality needed to detect changes based on a delta voltage at the sensor. Optimized for low-power applications, the LMP91200 works over a voltage range of 1.8 V to 5.5 V. With its extremely low input bias current it is optimized for use with pH sensors. Also, in absence of supply voltage the very low input bias current reduces degradation of the pH probe when connected to the LMP91200. Two guard pins provide support for high parasitic impedance wiring. Depending on the configuration, total current consumption for the device is 50 µA while measuring pH. Available in a 16-pin TSSOP package, the LMP91200 operates from –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP91200	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2015) to Revision E — **Page**

- Deleted SPI Function ... 1

Changes from Revision C (March 2013) to Revision D — **Page**

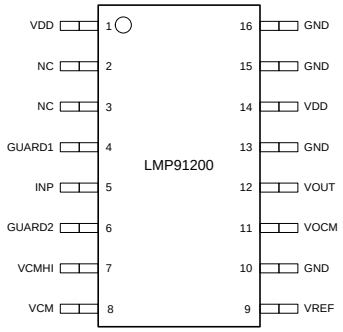
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted temperature sensor function. ... 1

Changes from Revision B (March 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format ... 17

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions (1)

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD	P	Positive Power Supply
2	NC	A	No connect. These pins should be left floating
3	NC	A	No connect. These pins should be left floating
4	GUARD1	A	Active guard pin
5	INP	A	Noninverting analog input of pH buffer
6	GUARD2	A	Active guard pin
7	VCMHI	A	High Impedance Common-Mode output
8	VCM	A	Buffered Common-Mode output
9	VREF	A	Voltage reference input
10	GND	G	Analog ground
11	VOCM	A	Output common-mode voltage
12	VOUT	A	Analog Output
13	GND	G	Connect to GND
14	VDD	P	Connect to VDD
15	GND	G	Connect to GND
16	GND	G	Connect to GND

(1) D = Digital, A = Analog, P = Power, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Supply Voltage (V_S = VDD – GND)	–0.3	6	V
Voltage between any two pins	–0.3	VDD + 0.3	V
Current out at any pin		5	mA
Junction Temperature(4)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications see product folder at www.ti.com and SNOA549.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		Machine Model	±150	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V_S = VDD – GND)	1.8	5.5	V
Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMP91200 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits specified for T_A = 25°C. V_S = (VDD – GND) = 3.3 V. VREF = 3.3 V.(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN(4)	TYP(5)	MAX(4)	UNIT
POWER SUPPLY							
Is	Supply Current(6)(7)	pH measurement mode			50	54	µA
			at the temperature extremes			59	
pH BUFFER							
Aol_{pH}	Open-loop Gain	INP = 1.65 V, 300 mV = VOUT = VDD – 300 mV			120		dB
			at the temperature extremes	90			
Vos_{pH}	Input Voltage Offset(6)	INP = 1/2 VREF		–200		200	µV
			at the temperature extremes	–350		350	
$TcVos_{pH}$	Input offset voltage drift(8)(9)	INP = 1/2 VREF		–2.5		2.5	uV/°C
VOS_{pH_drift}	Long-term V_{OSpH} drift(10)	500 hours OPL			150		µV
Ib_{pH}	Input bias current at INP(9)	0 V < INP < 3.3 V		–125		125	fA
		0 V < INP < 3.3 V, 85°C		–445		445	fA
		0 V < INP < 3.3 V, 125°C		–1.5		1.5	pA
		–500 mV < (INP – VCM) < 500 mV, V_S = 0 V.		–600		600	fA
		–500 mV < (INP – VCM) < 500 mV, 85°C, V_S = 0 V.		–6.5		6.5	pA
		–500 mV < (INP – VCM) < 500 mV, 125°C, V_S = 0 V.		–100		100	pA
$GBWP_{pH}$	Gain Bandwidth Product(9)	C_L = 10 pF, R_L = 1 MΩ			220		KHz
$CMRR_{pH}$	DC_Common-mode rejection ratio	INP = 1/2 VREF		80			dB
$PSRR_{pH}$	DC_Power supply rejection ratio	1.8 V < VDD < 5 V INP = 1/2 VREF		80			dB
En_RMS_{pH}	Input referred noise (low frequency)(9)	Integrated 0.1 Hz to 10 Hz			2.6		$µV_{PP}$
en_{pH}	Input referred noise (high frequency)(9)	f = 1 kHz			90		$nV/\sqrt{Hz}$
Isc_{pH}	Output short circuit current(11)	Sourcing, Vout to GND, INP = 1.65 V			13		mA
			at the temperature extremes	10			
		Sinking, Vout to VDD, INP = 1.65 V			12		mA
			at the temperature extremes	8			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Positive current corresponds to current flowing into the device.
(3) The voltage on any pin should not exceed 6 V relative to any other pins.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(6) Boldface limits are production tested at 125°C. Limits are specified through correlations using the Statistical Quality Control (SQC) method.
(7) Excluding all currents which flows out from the device.
(8) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(9) This parameter is specified by design and/or characterization and is not tested in production.
(10) Offset voltage long term drift is determined by dividing the change in V_{OS} at time extremes of OPL procedure by the length of the OPL procedure. OPL procedure: 500 hours at 150°C are equivalent to about 15 years.
(11) The short circuit test is a momentary open-loop test.

Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_A = 25°C. V_S = (VDD – GND) = 3.3 V. VREF = 3.3 V.[1][2][3]

PARAMETER		TEST CONDITIONS		MIN[4]	TYP[5]	MAX[4]	UNIT
VCM BUFFER							
VCMHI_acc	VCMHI accuracy			–1.6		1.6	mV
Tc_VCMHI	VCMHI temperature coefficient[9][12]	–40°C < T_A < 125°C		–18	–5	8	µV/°C
VCMHI_acc_VREF	VCMHI_acc vs. VREF[9][13]	1.8 V < VREF < 5 V		–500	–100	300	µV/V
$Rout_{VCMHI}$	VCMHI Output Impedance[9]	VCMHI = 1/2 VREF			250		KΩ
AoI_{VCM}	Open-loop Gain[6]	VCMHI = 1/2 VREF, 300 mV < VCM < VDD – 300 mV			120		dB
			at the temperature extremes	90			
Vos_{VCM}	(VCM – VCMHI)[6]	VCMHI = 1/2 VREF		–200		200	µV
			at the temperature extremes	–350		350	
$TcVos_{VCM}$	Input offset voltage drift (VCM-VCMHI)[8][9]	VCMHI = 1/2 VREF		–2.5		2.5	µV/°C
$Zout_{VCM}$	Output Impedance[9]	f = 1 KHz			4		Ω
$PSRR_{VCM}$	DC_Power supply rejection ratio	1.8 V < VDD < 5 V, VCMHI = 1/2 VREF		80			dB
En_RMS_{VCM}	Input referred noise (low frequency)[9]	Integrated 0.1 Hz to 10 Hz			2.6		$µV_{PP}$
en_{VCM}	Input referred noise (high frequency)[9]	f = 1 KHz			90		$nV/\sqrt{Hz}$
Isc_{VCM}	Output short circuit current[11]	Sourcing, Vout to GND VCMHI = 1/2 VREF			16		mA
			at the temperature extremes	10			
		Sinking, Vout to VDD VCMHI = 1/2 VREF			12		
			at the temperature extremes	8			

(12) VCMHI voltage average drift is determined by dividing the change in VCMHI at the temperature extremes by the total temperature change.
(13) VCMHI_acc vs. VREF is determined by dividing the change in VCMHI_acc at the VREF extremes by the total VREF change.

Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_A = 25°C. V_S = (VDD – GND) = 3.3 V. VREF = 3.3 V.[1][2][3]

PARAMETER		TEST CONDITIONS		MIN[4]	TYP[5]	MAX[4]	UNIT
PGA							
Vos_{PGA}	Input Voltage Offset[6]	+IN_PGA (Internal node) = 500 mV		–275		275	µV
			at the temperature extremes	–480		480	
$TcVos_{PGA}$	Input offset voltage drift[9][8]	+IN_PGA (Internal node) = 500 mV		–2.5		2.5	uV/°C
AoI_{PGA}	Open loop Gain	+IN_PGA (Internal node) = 500 mV			120		dB
			at the temperature extremes	90			
Av_{PGA}	Gain				5		V/V
Av_acc_{PGA}	Gain accuracy	at the temperature extremes		-1.3%		1.3%	
En_RMS_{PGA}	Input referred noise (low frequency)[9]	Integrated 0.1 Hz to 10 Hz			2.6		μV_{PP}
en_{PGA}	Input referred noise (high frequency)[9]	f = 1 kHz			90		$nV/\sqrt{Hz}$
$PSRR_{PGA}$	DC_Power supply rejection ratio	1.8 V < VDD < 5 V, +IN_PGA (Internal node) = 500 mV		80			dB
Isc_{PGA}	Output short circuit current[11]	Sourcing, Vout to GND +IN_PGA (Internal node) = 500 mV			16		mA
			at the temperature extremes	10			
		Sinking, Vout to VDD +IN_PGA (Internal node) = 500 mV			12		
			at the temperature extremes	8			
REFERENCE INPUT							
Rin_{VREF}	Input impedance[9]				500		KΩ

6.6 Typical Characteristics

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

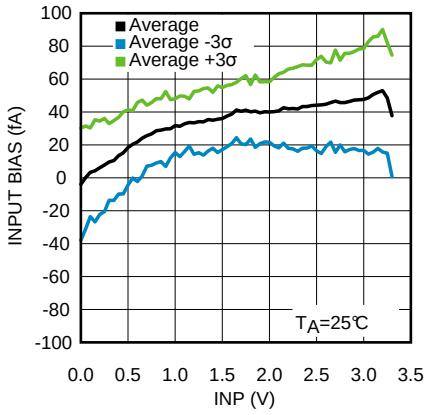


Figure 1. pH Buffer Input Bias Current vs V_{INP} - Device ON

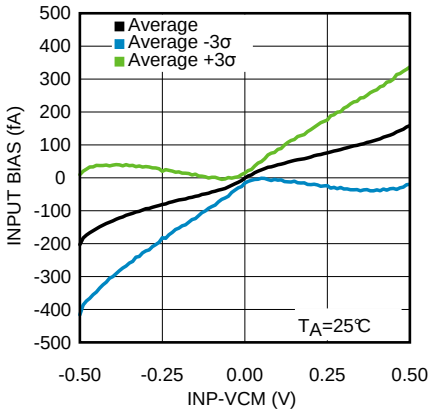


Figure 2. pH Buffer Input Bias Current vs V_{INP} - Device OFF

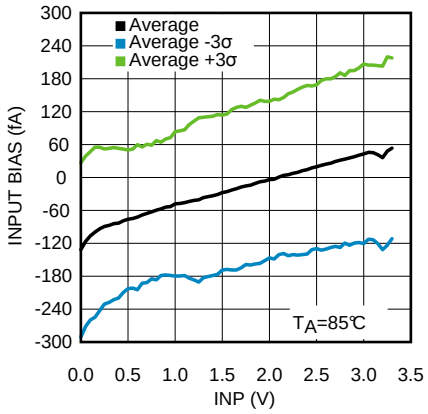


Figure 3. pH Buffer Input Bias Current vs V_{INP} - Device ON

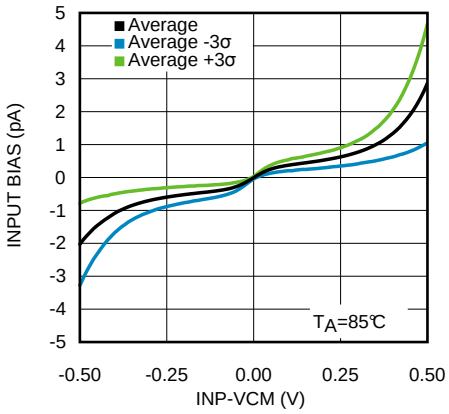


Figure 4. pH Buffer Input Bias Current vs V_{INP} - Device OFF

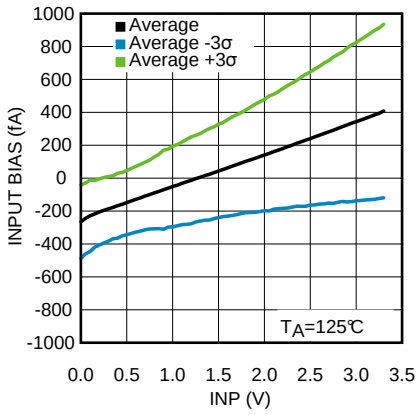


Figure 5. pH Buffer Input Bias Current vs V_{INP} - Device ON

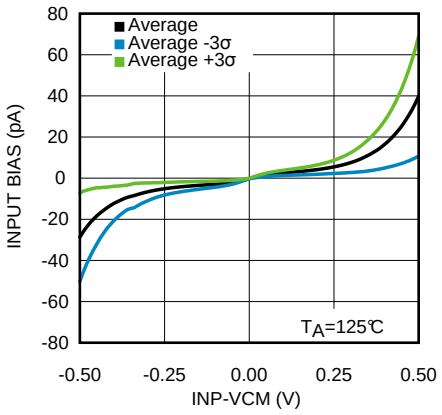


Figure 6. pH Buffer Input Bias Current vs V_{INP} - Device OFF

Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

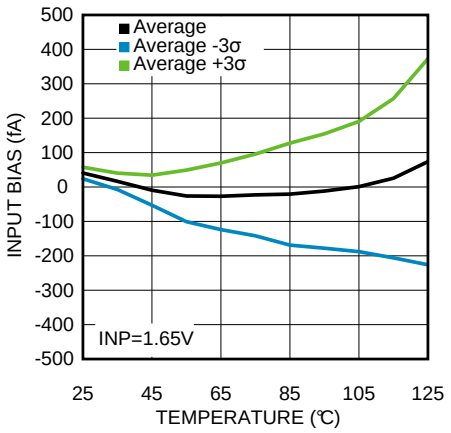


Figure 7. pH Buffer Input Bias Current vs Temp - Device ON

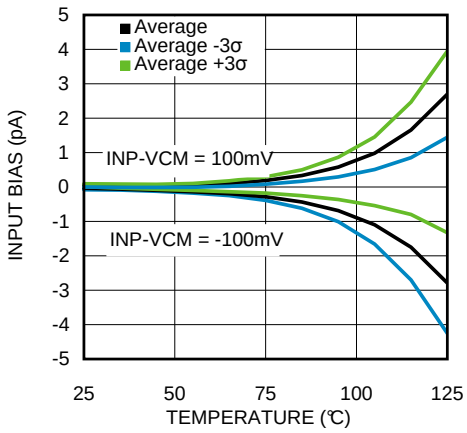


Figure 8. pH Buffer Input Bias Current vs Temp - Device OFF

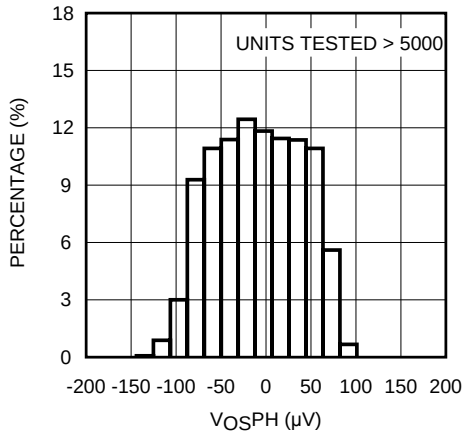


Figure 9. pH Buffer Input Voltage Offset

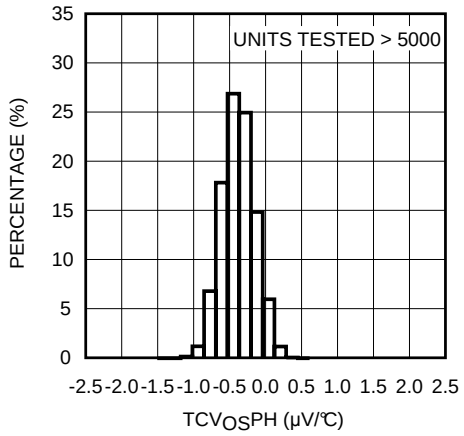


Figure 10. pH Buffer TCV_{OS}

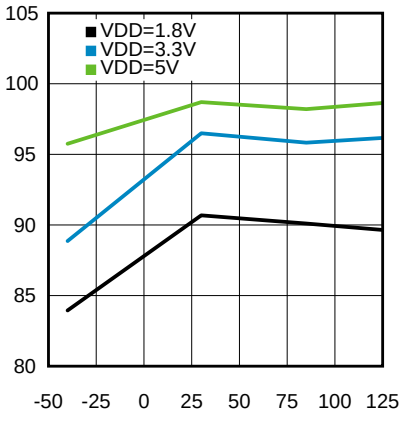


Figure 11. pH Buffer DC CMRR vs Temperature

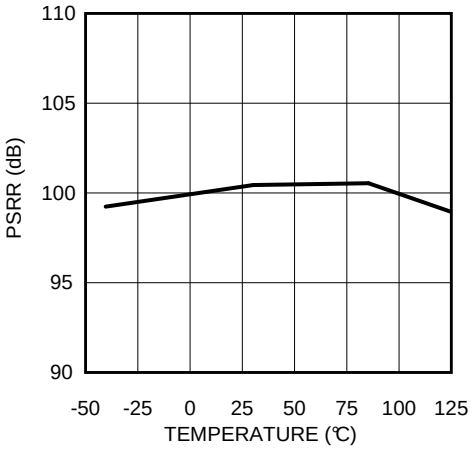


Figure 12. pH Buffer DC PSRR vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

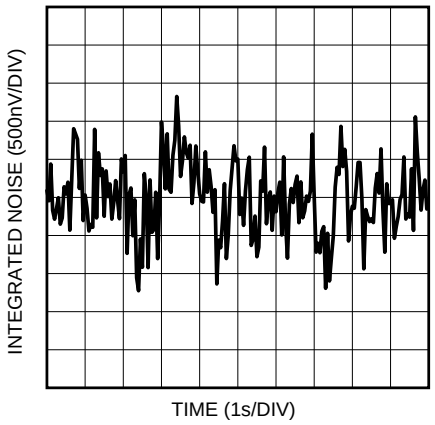


Figure 13. pH Buffer Time Domain Voltage Noise

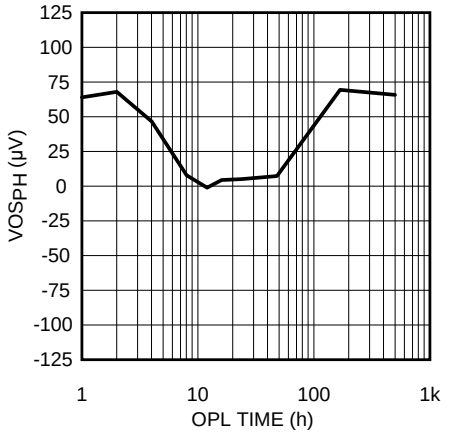


Figure 14. pH Buffer Input Offset Voltage Drift

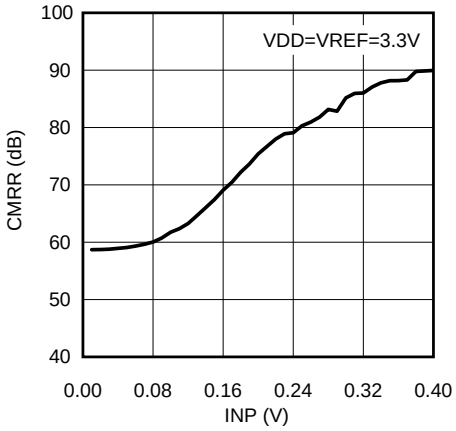


Figure 15. pH Buffer CMRR vs V_{INP} - Lower Rail

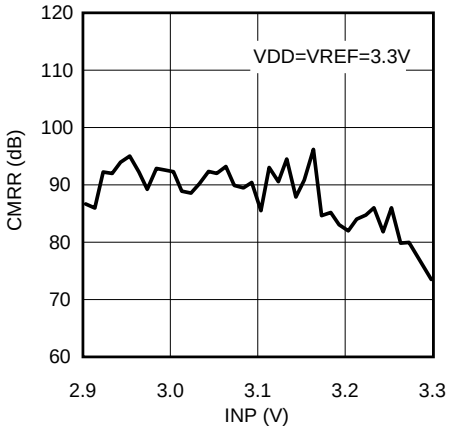


Figure 16. pH Buffer CMRR vs V_{INP} - upper rail

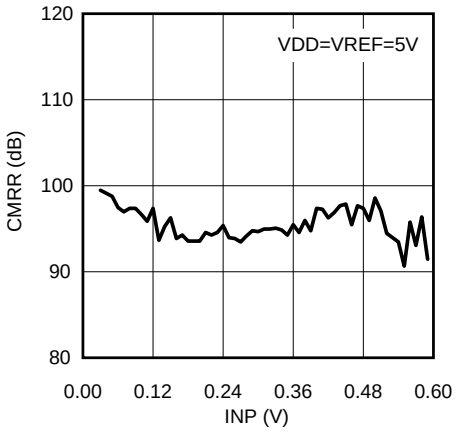


Figure 17. pH Buffer CMRR vs V_{INP} - lower rail

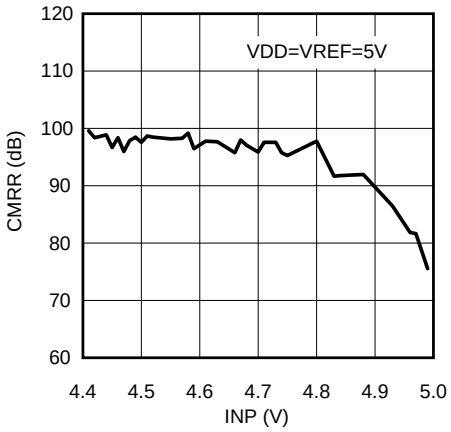


Figure 18. pH Buffer CMRR vs V_{INP} - upper rail

Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

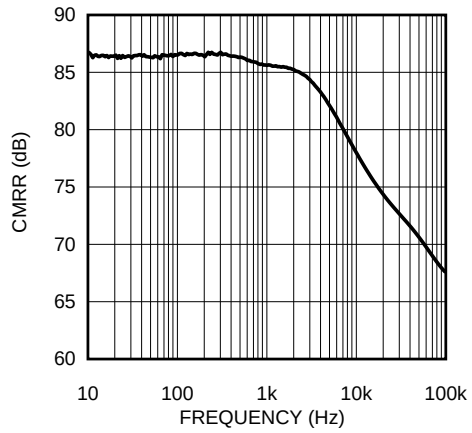


Figure 19. pH Buffer CMRR vs Frequency

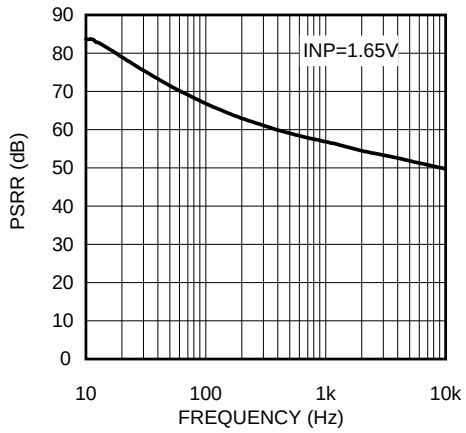


Figure 20. pH Buffer PSRR vs Frequency

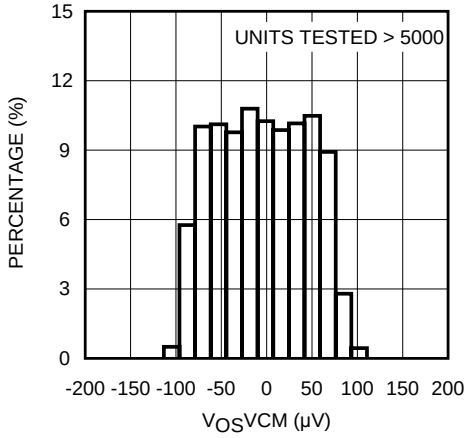


Figure 21. VCM Buffer Input Voltage Offset

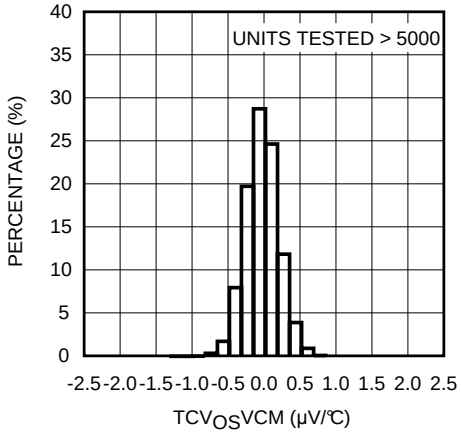


Figure 22. VCM Buffer TCV_{OS}

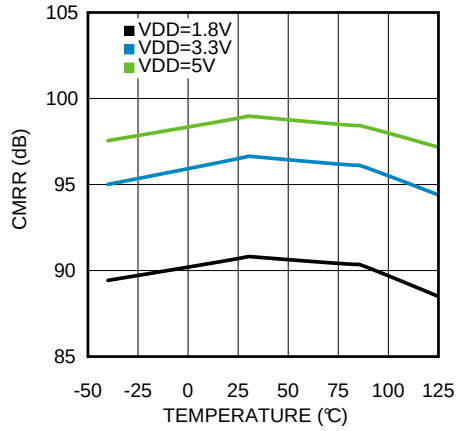


Figure 23. VCM Buffer DC CMRR vs Temperature

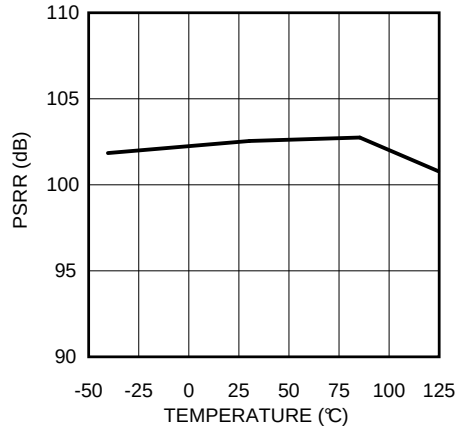


Figure 24. VCM Buffer DC PSRR vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

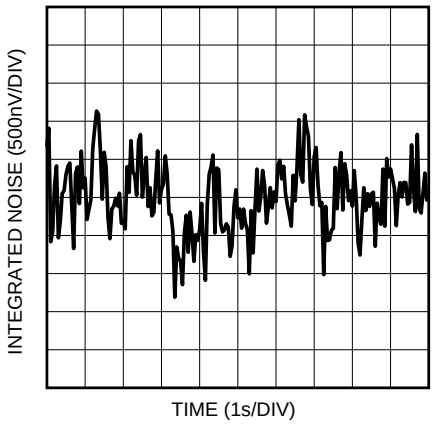


Figure 25. VCM Buffer Time Domain Voltage Noise

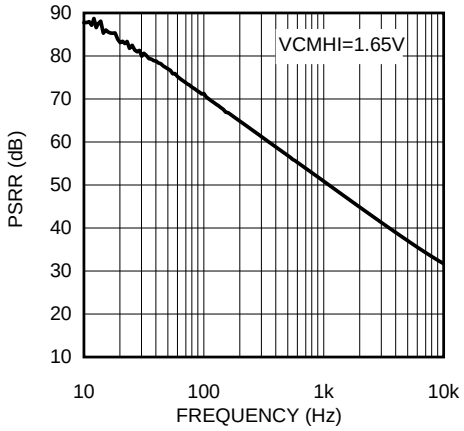


Figure 26. VCM Buffer PSRR vs Frequency

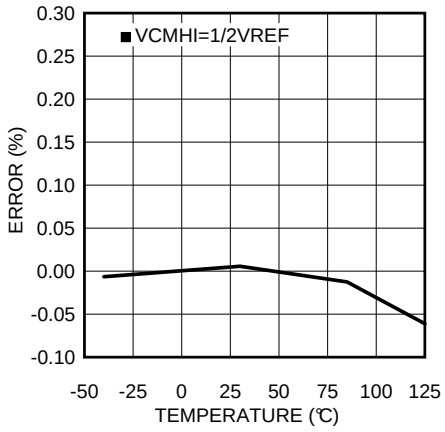


Figure 27. VCMHI Error vs Temp

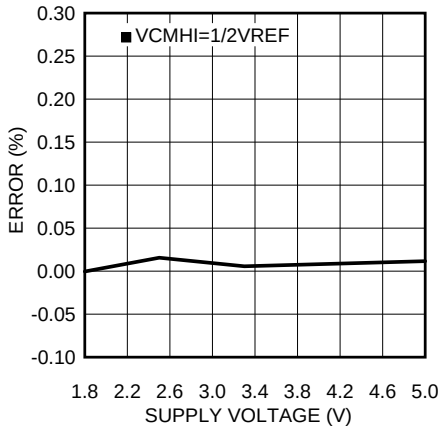


Figure 28. VCMHI Error vs Supply Voltage

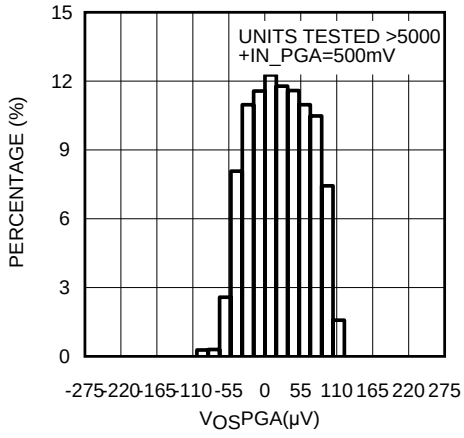


Figure 29. PGA Input Voltage Offset

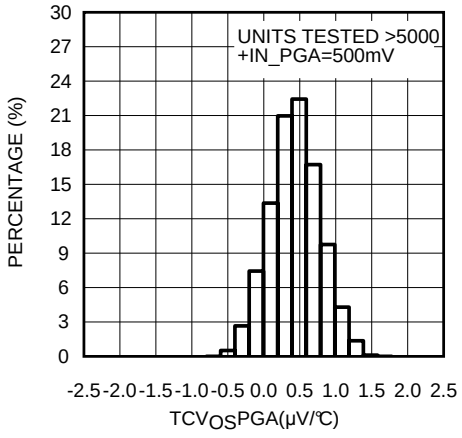


Figure 30. PGA TCV_{OS}

Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= (VDD – GND) = 3.3 V, VREF = 3.3 V.

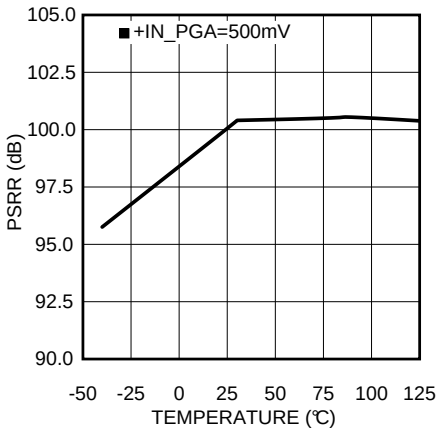


Figure 31. PGA DC PSRR vs Temperature

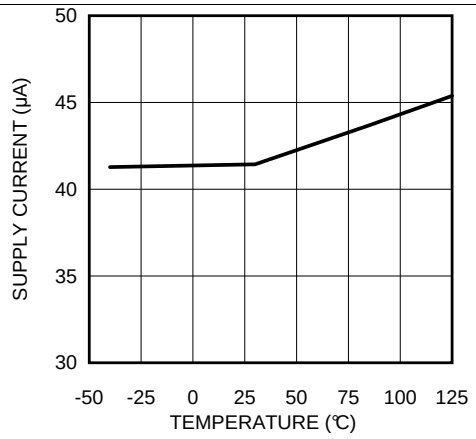


Figure 32. Supply Current vs Temperature

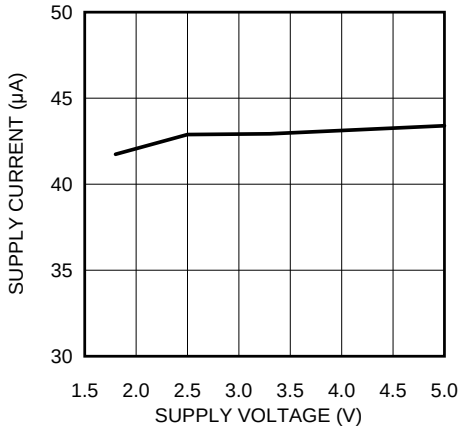


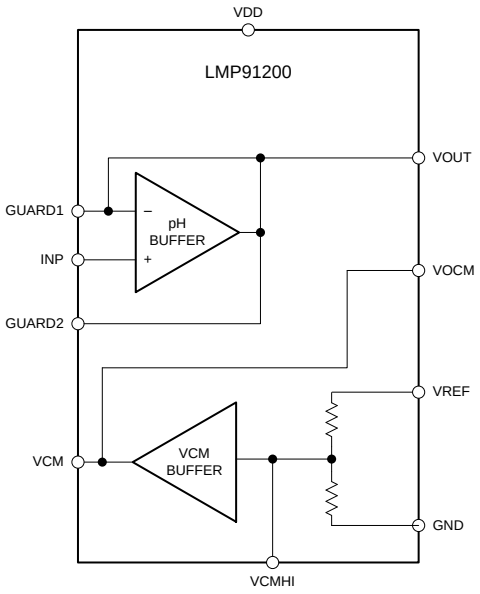
Figure 33. Supply Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The LMP91200 is a sensor AFE for use in low-power, analytical-sensing applications. The LMP91200 is designed for 2-electrode sensors. This device provides all of the functionality needed to detect changes based on a delta voltage at the sensor. Optimized for low-power applications, the LMP91200 works over a voltage range of 1.8 V to 5.5 V. With its extremely low input bias current, it is optimized for use with pH sensors. Also, in the absence of supply voltage, the very low input bias current reduces degradation of the pH probe when connected to the LMP91200. Two guard pins provide support for high parasitic impedance wiring.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 pH Buffer

The pH Buffer is a unity gain buffer with a input bias current in the range of tens fA at room temperature. Its very low bias current introduces a negligible error in the measurement of the pH. The ph buffer is provided with 2 guard pins (GUARD1, GUARD2) in order to minimize the leakage of the input current and to make the design of a guard ring easy.

7.3.2 VCM Buffer

Both buffered and unbuffered version of the common-mode voltage are available respectively at the VCM pin and VCMHI pin. A copy of the buffered version is present at VOCM pin in case of differential measurement.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Theory of pH Measurement

The pH electrode measurements are made by comparing the readings in a sample with the readings in standards whose pH has been defined (buffers). When a pH sensing electrode comes in contact with a sample, a potential develops across the sensing membrane surface and that membrane potential varies with pH. A reference electrode provides a second, unvarying potential to quantitatively compare the changes of the sensing membrane potential. These days, pH electrodes are composed of a sensing electrode with the reference electrode built into the same electrode body, and they are called combination electrodes. A high input impedance meter serves as the readout device and calculates the difference between the reference electrode and sensing electrode potentials in millivolts. The millivolts are then converted to pH units according to the Nernst equation.

Electrode behavior is described by the Nernst equation:

$$E = Eo + (2.3\ RT/nF) \log aH+ \quad (1)$$

where

- E is the measured potential from the sensing electrode,
- Eo is related to the potential of the reference electrode,
- (2.3 RT/nF) is the Nernst factor,
- log aH+ is the pH, (aH+ = activity of Hydrogen ions).

2.3 RT/nF includes the Gas Law constant (R), Faraday's constant (F), the temperature in degrees Kelvin (T) and the stoichiometric number of ions involved in the process (n). For pH, where n = 1, the Nernst factor is 2.3 RT/F. Because R and F are constants, the factor and therefore electrode behavior is dependent on temperature. The Nernst Factor is equivalent to the electrode slope which is a measure of the electrode response to the ion being detected. When the temperature is 25°C, the theoretical Nernst slope is 59.16 mV/pH unit.

8.2 Typical Application

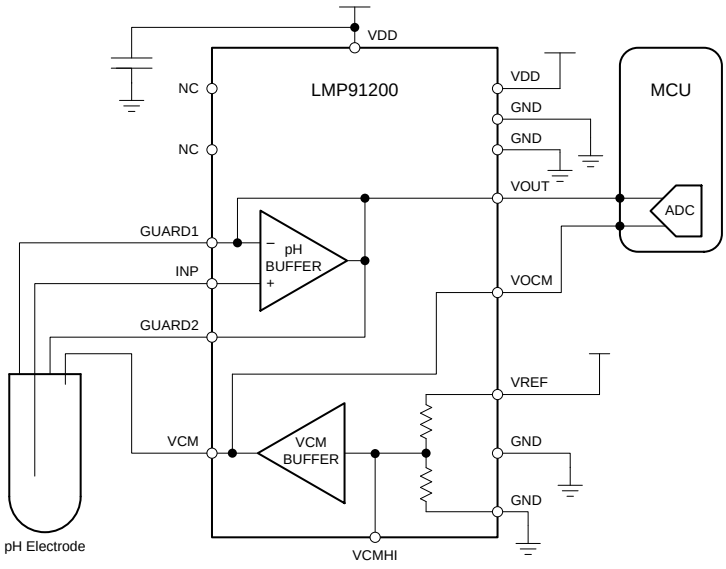


Figure 34. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

8.2.1.1 pH Measurement

The output of a pH electrode ranges from 415 mV to −415 mV as the pH changes from 0 to 14 at 25°C. The output impedance of a pH electrode is extremely high, ranging from 10 MΩ to 1000 MΩ. The low input bias current of the LMP91200 allows the voltage error produced by the input bias current and electrode resistance to be minimal. For example, if the output impedance of the pH electrode used is 10 MΩ and an operational amplifier with 3 nA of Ibias is used, the error caused due to the input bias current of the amplifier and the source resistance of the pH electrode is 30 mV! This error can be greatly reduced to 1.25 µV by using the LMP91200.

The pH measurement with the LMP91200 is straightforward. The pH electrode must be connected between the VCM pin and the INP pin. The voltage at the VCM pin represents the internal zero of the system so the potential of the electrode (voltage at INP pin) will be referred to the VCM voltage.

8.2.2 Detailed Design Procedure

The LMP91200 is configured to execute a pH measurement as described in the *pH Measurement* section.

8.2.3 Application Curves

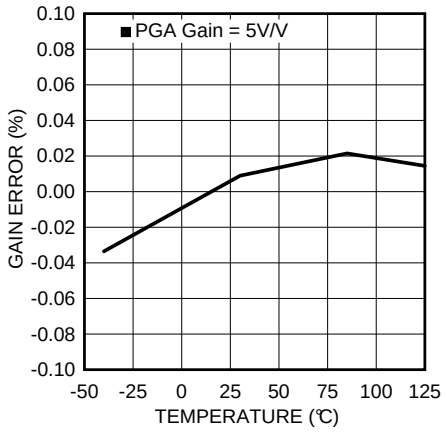


Figure 35. PGA Gain Error vs Temp

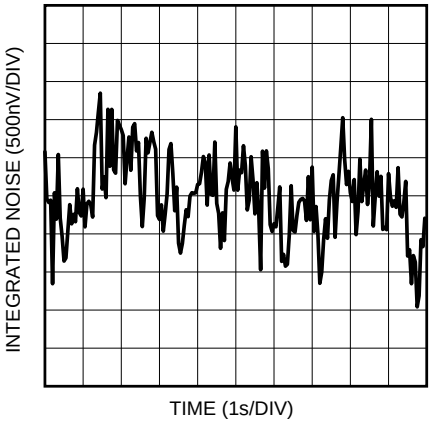


Figure 36. PGA Time Domain Voltage Noise

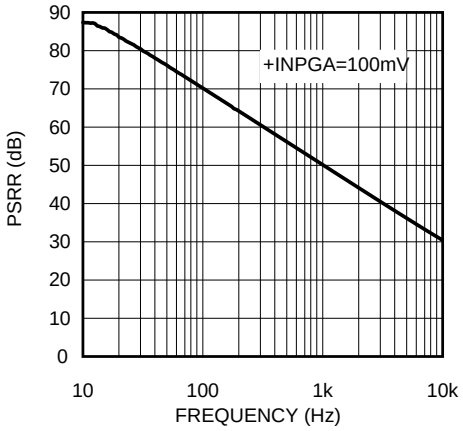


Figure 37. PGA PSRR vs Frequency

9 Power Supply Recommendations

VDD should be bypassed with 10-µF, 1-µF and 0.1-µF capacitors, placed as close as possible to the LMP91200 VDD pin (pin 1). An LDO is recommended for the supply rail, but a DC-DC switcher may be used if sufficient filtering is used to attenuate the switching frequency components.

10 Layout

10.1 Layout Guidelines

Due to the high impedance of the ph Electrode in the pH measurement, careful circuit layout and assembly are required. Guarding techniques are highly recommended to reduce parasitic leakage current by isolating the input of the LMP91200 from large voltage gradients across the PCB. A guard is a low impedance conductor that surrounds an input line and its potential is raised to the voltage of the input line. The input pin should be fully guarded as shown in Figure 38. The guard traces should completely encircle the input connections. In addition, they should be located on both sides of the PCB and be connected together. The LMP91200 makes the guard ring easy to be implemented without any other external operational amplifier. The ring needs to be connected to the guard pins (GUARD1 and GUARD2), which are at the same potential as that of the INP pin. Solder mask should not cover the input and the guard area, including guard traces on either side of the PCB. Sockets are not recommended as they can be a significant leakage source. After assembly, a thorough cleaning using commercial solvent is necessary.

Figure 38 shows a typical guard ring circuit when the LMP912000 is interfaced to a pH probe through a triaxial cable/connector (usually referred to as *triax*). The signal conductor and the guard of the triax should be kept at the same potential. Therefore, the leakage current between them is practically zero. Because the triax has an extra layer of insulation and a second conducting sheath, it offers greater rejection of interference than coaxial cable or connector.

10.2 Layout Example

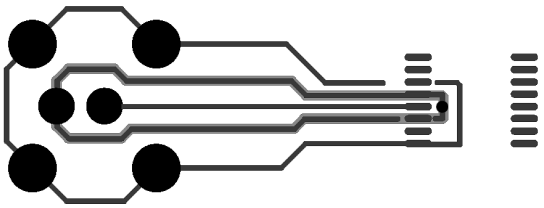


Figure 38. Circuit Board Guard Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP91200MT/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP912 00MT	Samples
LMP91200MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP912 00MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

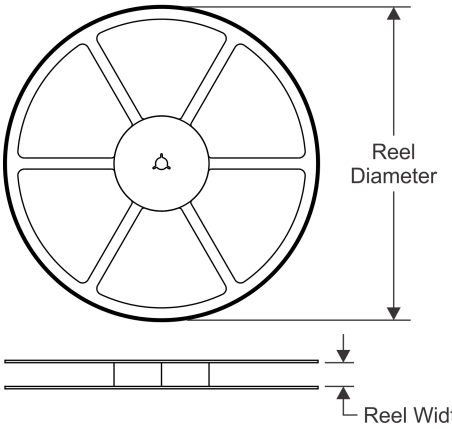
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

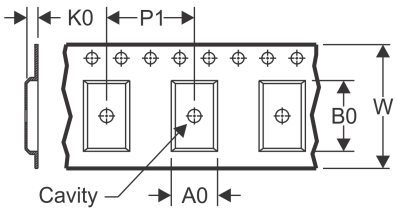
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

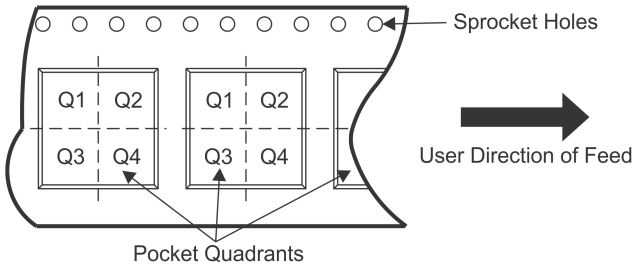


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

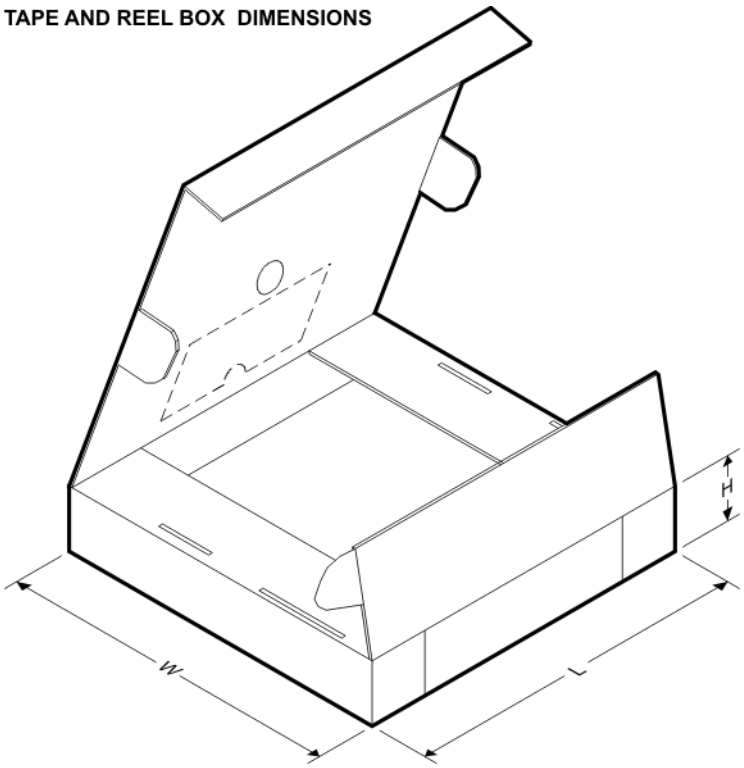
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91200MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

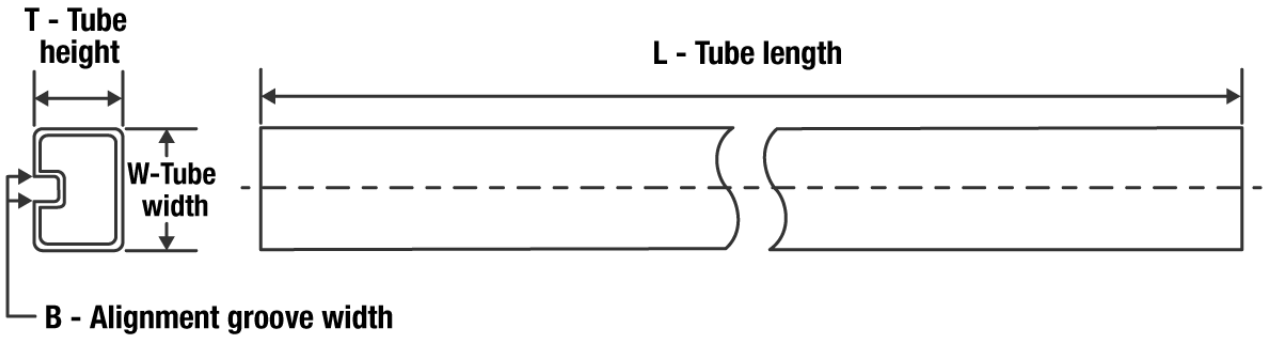
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP91200MTX/NOPB	TSSOP	PW	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

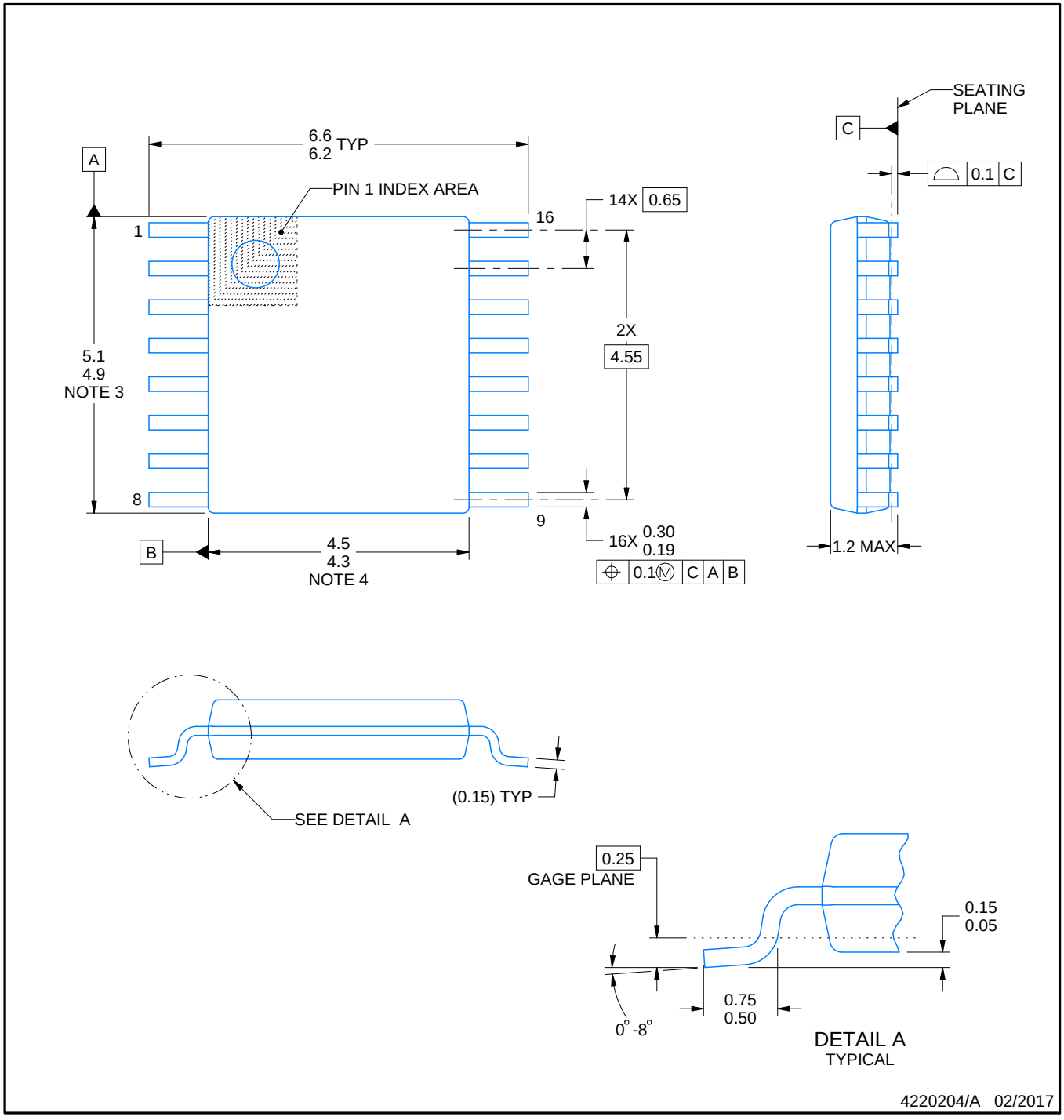
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP91200MT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

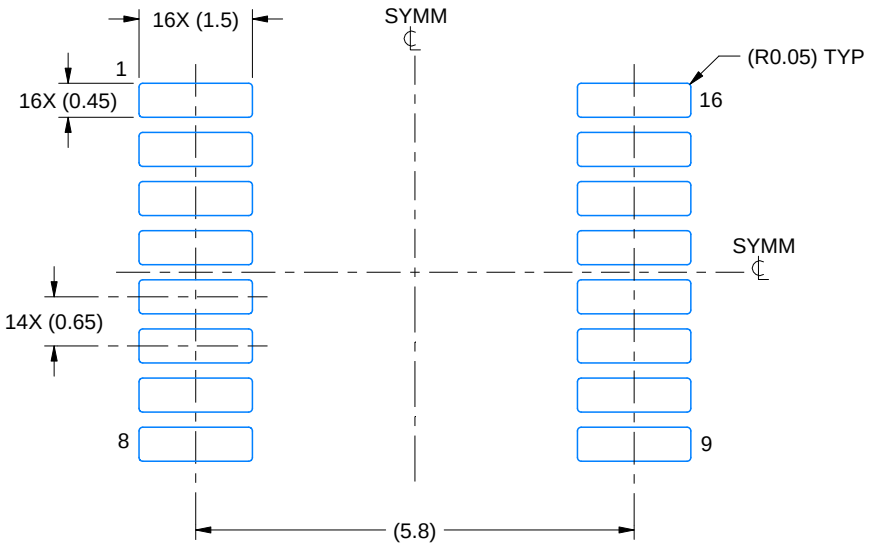
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

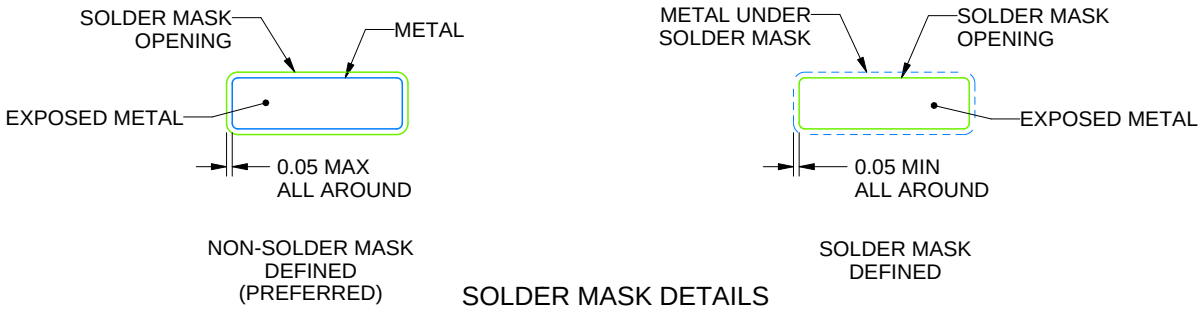


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

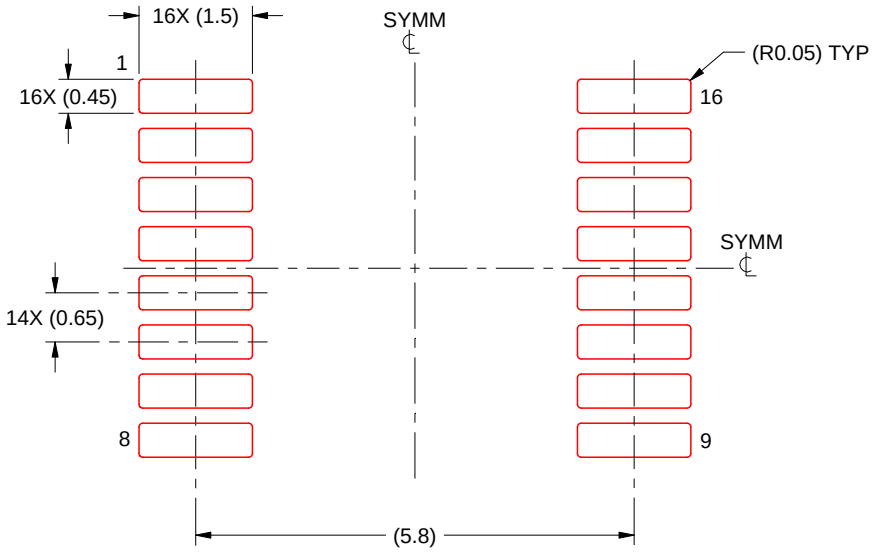


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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