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APPLICATION NOTE 3662

Understanding LVDS Fail-Safe Circuits

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Abstract: Low-voltage differential signaling (LVDS) is a widely used differential signaling technology for high-speed digital-signal interconnections. In many applications, the LVDS receiver needs a fail-safe function to avoid an uncertain output state when the input is connected improperly. In this application note, we will examine the circuit design and performance characteristics of three popular fail-safe functions. Comparative analysis of circuit designs will guide readers in the use of fail-safe circuits for high-speed data-transfer applications.

Introduction

In recent years low-voltage differential signaling (LVDS)[1] for high-speed data interconnections has found broad application in consumer electronics, high-speed computer peripherals, telecom/networking, and wireless base stations. LVDS has distinctive advantages in performance, power, noise, EMI reduction, and cost. With appropriate settings, at a data rate of 100Mbps to 800Mbps the LVDS signal can reach as far as 10m to 15m in a twisted-pair cable link, or > 1m in a PCB trace pair. The power dissipated by the 100Ω load is a mere 1.2mW relatively independent of frequency.

This application note discusses the LVDS fail-safe function, which is very important for appropriate LVDS operation. We will examine three fail-safe circuits, analyze their characteristics, and provide guidance for applications.

Basic Characteristics and Advantages of LVDS

Let us briefly review the basic structure of the LVDS signaling and circuit configuration. **Figure 1** shows a simple, basic circuit for LVDS transmission and receiving. The receiver is a comparator with an absolute transition threshold of about 50mV. The transmission media, whether cable or PCB trace pair, are designed with a 100Ω differential impedance. **Figure 2** shows the signal levels for both common and differential modes on the media. In Figures 1 and 2, V_{ID} is the input differential voltage of the LVDS receiver, V_{OD} is the differential output voltage of the LVDS transmitter, and V_{CM} is the common-mode voltage.

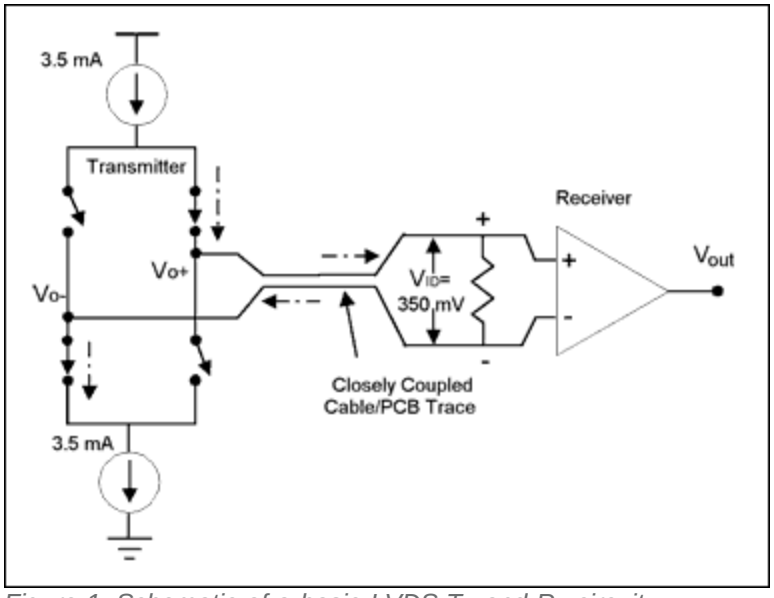

Figure 1. Schematic of a basic LVDS Tx and Rx circuit.

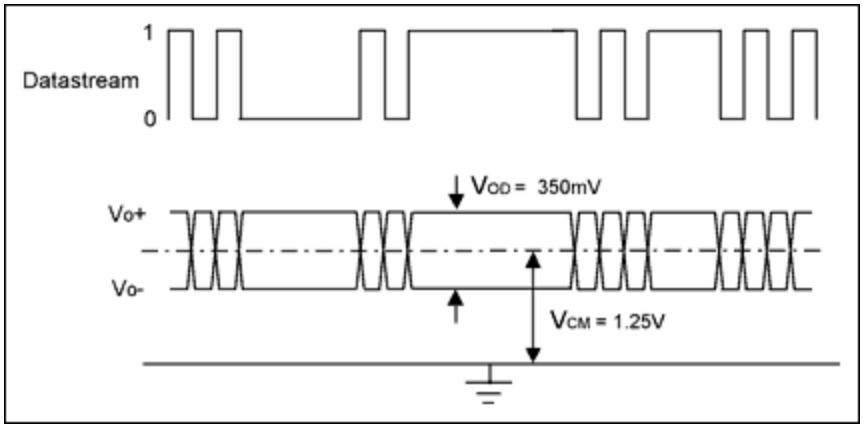

Figure 2. Common and differential modes of LVDS signaling.

With a current source constantly driving the two closely coupled wires or traces, the common-mode current and voltage on the medium do not vary in time, regardless of the changes on the differential mode. In general, the data transmitting speed is limited principally by the parasitic capacitance and inductance on its load. For the LVDS circuit shown in Figure 1, most of the loading capacitance presents common-mode impedance to the driver (transmitter). On the other hand, most of the inductance comes from the chip or load leads, not from the matched transmission line. Moreover, the value of the parasitic inductance is relatively small, causing negligible effect on signal integrity. Because the common-mode voltage is unchanged on the load, most of the effects from the load parasitic capacitance are eliminated. Consequently, LVDS runs at a much higher data rate than CMOS or TTL signals.

Because the coupling of the two wires or traces is so close, only the common mode affects EMI. The negligible common-mode variation during transmission means that LVDS has a very low radiation level, even in very high-rate operations. Furthermore, with a 350mV low-differential voltage swing, the 100Ω termination only consumes 1.2mW which is constant and independent of the data rate. The low power consumption of LVDS is a significant difference from the higher power consumed by single-ended signaling such as CMOS and TTL.

Fail-Safe Function

Most LVDS receivers require internal or external fail-safe circuitry so that under a specific link condition or failure the receiver's output will have a known logic condition, usually logic-high. The following list shows the link conditions or failures that need the fail-safe function.

- Open inputs: if the LVDS chip has multiple receiver ports, the unused receiver inputs should be left open and the output should be a stable logic-high.
- Float inputs: if the LVDS driver is in tri-state, the driver is powered-off, or link is broken, the LVDS must have a stable logic-high output.
- Shorted inputs: if the two parallel LVDS wires or traces are shorted together, this is a fault connection and the logic-high output state needs to be asserted.

Designers also want a fail-safe function to be robust in noisy environments and have negligible effect on normal LVDS operation.

Fail-Safe Circuits and Performance Analysis

There are three basic types of fail-safe circuits: external-biasing circuit, in-path circuit, and parallel circuit. We will describe how each of these fail-safe circuits works, and then analyze their respective performance strengths and weaknesses.

External-Biasing Fail-Safe Circuit

This fail-safe function is a simple circuit consisting of three resistors connected externally to the receiver input pins (**Figure 3**).

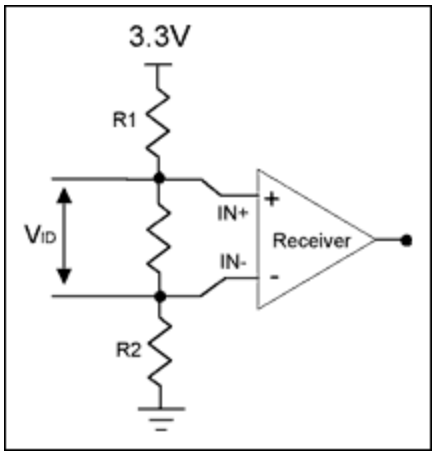

Figure 3. External fail-safe circuit.

In this design the biasing sets a positive offset voltage between the two input pins when the line is not driven so that the receiver's output is in a logic-high state. The offset value of V_{ID} is set according the following expression:

$$V_{ID(offset)} = \frac{100 \times V_{CC}}{R1 + R2 + 100}$$

The common-mode voltage of the circuit obeys the following relation:

$$V_{CM} = \frac{R2 + 50}{R1 + R2 + 100} V_{CC}$$

To have a 50mV offset on V_{ID} of a float line, for example, we can choose R1 = 4170Ω and R2 = 2450Ω. If we assume that the amplitude of the noise is less than the offset ofVID, then the receiver's output will be in a logic-high state.

This fail-safe circuit was widely used for the early generations of LVDS receivers. It was the preferred design for the following reasons:

- It offers the flexibility of setting the offset voltage externally according to the noise level on a float line.
- It provides a common-mode return path and a discharge path for ESD.

The design, however, has disadvantages that limit its use in current LVDS applications.

- The requirement for two external resistors may not be a burden for a single LVDS link, but can be a concern when multiple links are used, especially in multichannel applications.
- Today, the LVDS data rate can reach 800Mbps or even more than 2Gbps for computer peripheral and network interconnections. Under such a high-speed data transmission, the unbalanced receiver threshold created by the V_{ID} offset can cause considerable distortion on the duty cycle and increase jitter.
- It has a low noise margin on fail-safe for differential noise, because theVID offset cannot be set too high.
- This circuit does not work for the shorted-input fault. When the rail gets shorted, the V_{ID} offset voltage source is also shorted and the LVDS output is undetermined.

In-Path Fail-Safe Circuit

The in-path fail-safe design is similar to the external-biasing fail-safe approach, except that here R1 and R2 are integrated into LVDS receivers so the offset on V_{ID} is now a built-in voltage source. This circuit has been used extensively in some LVDS receivers[2]. An equivalent circuit is shown in **Figure 4**.

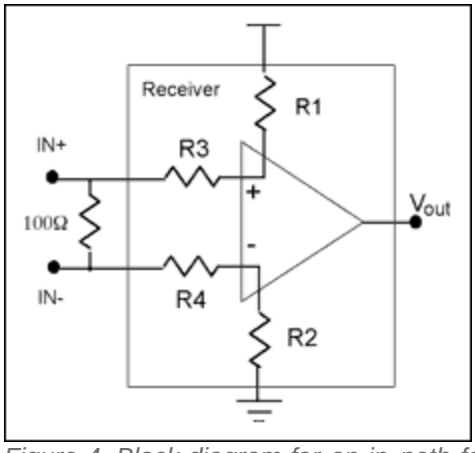

Figure 4. Block diagram for an in-path fail-safe circuit.

With an in-path circuit design, the R1 and R2 values are chosen so that the value of the internal offset of V_{ID} is between 30mV to 50mV. The positive V_{ID} offset is inserted even when the inputs are short, which puts the output to the high-state whenever the above three conditions require fail-safe protection.

This in-path design moves beyond the external-biasing method because it overcomes some of the latter's shortcomings. The in-path fail-safe circuit:

- Eliminates the external resistors.
- Functions when the inputs are shorted.

Nonetheless, the in-path fail-safe approach still has major drawbacks for some applications.

- It does not give the flexibility of setting the offset voltage.
- It causes an unbalanced receiver threshold, degrading duty cycle and increasing jitter.
- It has a low noise margin on 'in-path' noise.

Parallel Fail-Safe Circuit

This parallel fail-safe circuit is used in most of Maxim's LVDS products[3]. It overcomes the major drawbacks of the two prior fail-safe circuits and is illustrated in **Figure 5**.

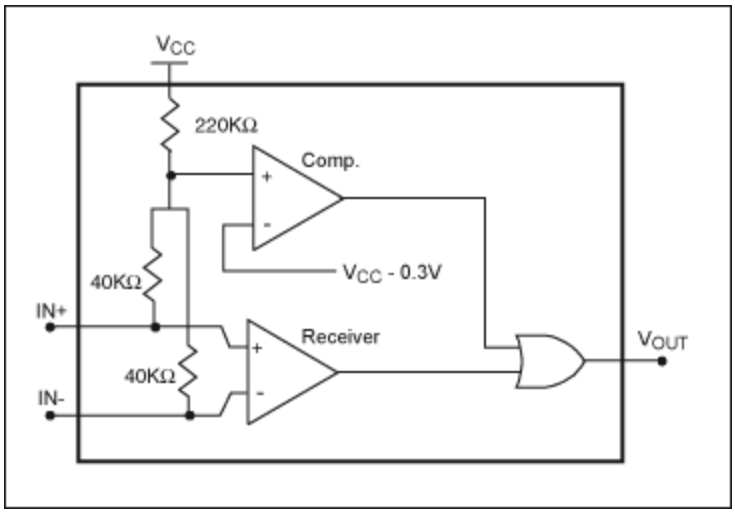

Figure 5. Schematic of a parallel fail-safe circuit.

As shown in Figure 5, the comparator monitors the voltage level on the rail and compares it with a reference of V_{CC} - 0.3V. If the rail voltage level is higher than the reference, its output goes to logic-high. Then this logic-high state blocks the receiver's output through an OR gate and the fail-safe function is activated. This configuration can pull the LVDS output to logic-high in the three scenarios requiring the fail-safe function listed earlier: open, float, and short. This functional design can work properly as long as the common-mode voltage is less than the reference voltage, V_{CC} - 0.3V.

The parallel fail-safe method provides some unique advantages over both older methods.

- It has a much higher noise margin for both the common and differential modes.
- Its configuration is symmetrical and has no degradation on the duty cycle and jitter of the input differential signal.

Despite its unique benefits, there is a concern with using this parallel method. For multipoint or long-distance point-to-point applications, the common loading capacitance could be relatively large. When a failure occurs, this circuit will take some time for charging the common-mode voltage level to V_{CC} - 0.3V. This, in turn, adds an activation delay to the fail-safe function.

Summary

This application note discusses the design, operation, strengths and shortcomings of three different fail-

safe circuits: external-biasing, in-path, and parallel circuits. We saw that there is no single all-perfect solution for an LVDS fail-safe function. The analysis shows, however, that the parallel method can work well in more situations than either of the other two methods.

References

[1] IEEE Std 1596.3-1996 IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) (PDF)
[2] Data sheets of DC36C200, DS90C032, and DS90LV018
[3] Maxim LVDS Line Drivers/Receivers

Related Parts		
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