



**256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs
2.5V I/O, Burst Counter
Pipelined Outputs**

**IDT71V65602/Z
IDT71V65802/Z**

Features

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high performance system speed - 150MHz (3.8ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control \overline{OE}
- ◆ Single R/\overline{W} (READ/WRITE) control pin
- ◆ Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- ◆ 4-word burst capability (interleaved or linear)
- ◆ Individual byte write (\overline{BW}_1 - \overline{BW}_4) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 3.3V power supply ($\pm 5\%$)
- ◆ 2.5V I/O Supply (V_{DDO})
- ◆ Power down controlled by ZZ input
- ◆ Packaged in a JEDEC standard 100-pin plastic thin quad and flatpack (TOFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (FBGA)

Description

The IDT71V65602/5802 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V65602/5802 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable (\overline{CEN}) pin allows operation of the IDT71V65602/5802 to be suspended as long as necessary. All synchronous inputs are ignored when (\overline{CEN}) is high and the internal device registers will hold their previous values.

There are three chip enable pins (\overline{CE}_1 , CE_2 , \overline{CE}_2) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/\overline{LD} is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71V65602/5802 have an on-chip burst counter. In the burst mode, the IDT71V65602/5802 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the \overline{LBO} input pin. The \overline{LBO} pin selects between linear and interleaved burst sequence. The ADV/\overline{LD} signal is used to load a new external address ($ADV/\overline{LD} = \text{LOW}$) or increment the internal burst counter ($ADV/\overline{LD} = \text{HIGH}$).

The IDT71V65602/5802 SRAM utilize IDT's latest high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TOFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (FBGA).

Pin Description Summary

| | | | |
|---|--|--------|--------------|
| A0-A18 | Address Inputs | Input | Synchronous |
| \overline{CE}_1 , CE_2 , \overline{CE}_2 | Chip Enables | Input | Synchronous |
| \overline{OE} | Output Enable | Input | Asynchronous |
| R/\overline{W} | Read/Write Signal | Input | Synchronous |
| \overline{CEN} | Clock Enable | Input | Synchronous |
| \overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , \overline{BW}_4 | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| ADV/\overline{LD} | Advance burst address / Load new address | Input | Synchronous |
| \overline{LBO} | Linear / Interleaved Burst Order | Input | Static |
| ZZ | Sleep Mode | Input | Asynchronous |
| I/O0-I/O31, I/OP1-I/OP4 | Data Input / Output | I/O | Synchronous |
| V_{DD} , V_{DDO} | Core Power, I/O Power | Supply | Static |
| V_{SS} | Ground | Supply | Static |

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Pin Definitions⁽¹⁾

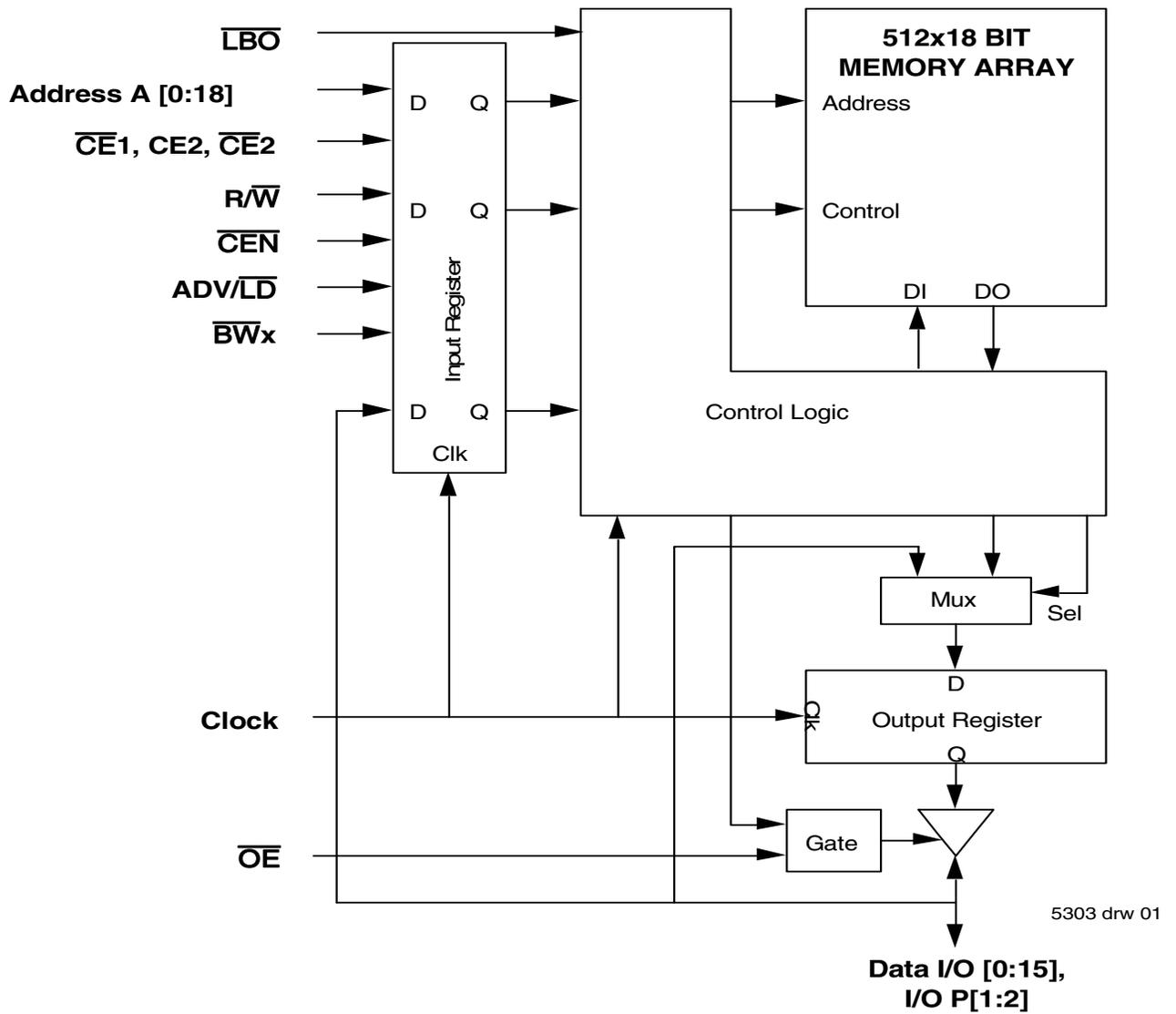
| Symbol | Pin Function | I/O | Active | Description |
|---------------------------|-------------------------------|-----|--------|--|
| A0-A18 | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, CEN low, and true chip enables. |
| ADV/LD | Advance / Load | I | N/A | ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high. |
| R/W | Read / Write | I | N/A | R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later. |
| CEN | Clock Enable | I | LOW | Synchronous Clock Enable Input. When CEN is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CEN sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, CEN must be sampled low at rising edge of clock. |
| BW1-BW4 | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal (BW1-BW4) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BW1-BW4 can all be tied low if always doing write to the entire 36-bit word. |
| CE1, CE2 | Chip Enables | I | LOW | Synchronous active low chip enable. CE1 and CE2 are used with CE2 to enable the IDT71V65602/5802. (CE1 or CE2 sampled high or CE2 sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated. |
| CE2 | Chip Enable | I | HIGH | Synchronous active high chip enable. CE2 is used with CE1 and CE2 to enable the chip. CE2 has inverted polarity but otherwise identical to CE1 and CE2. |
| CLK | Clock | I | N/A | This is the clock input to the IDT71V65602/5802. Except for OE, all timing references for the device are made with respect to the rising edge of CLK. |
| I/O0-I/O31 I/OP1-I/OP4 | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| LBO | Linear Burst Order | I | LOW | Burst order selection input. When LBO is high the Interleaved burst sequence is selected. When LBO is low the Linear burst sequence is selected. LBO is a static input and it must not change during device operation. |
| OE | Output Enable | I | LOW | Asynchronous output enable. OE must be low to read data from the IDT71V65602/5802. When OE is high the I/O pins are in a high-impedance state. OE does not need to be actively controlled for read and write cycles. In normal operation, OE can be tied low. |
| ZZ | Sleep Mode | I | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down 71V65602/5802 to the lowest power consumption level. Data retention is guaranteed in Sleep Mode. |
| VDD | Power Supply | N/A | N/A | 3.3V core power supply. |
| VDDO | Power Supply | N/A | N/A | 2.5V I/O Supply. |
| VSS | Ground | N/A | N/A | Ground. |

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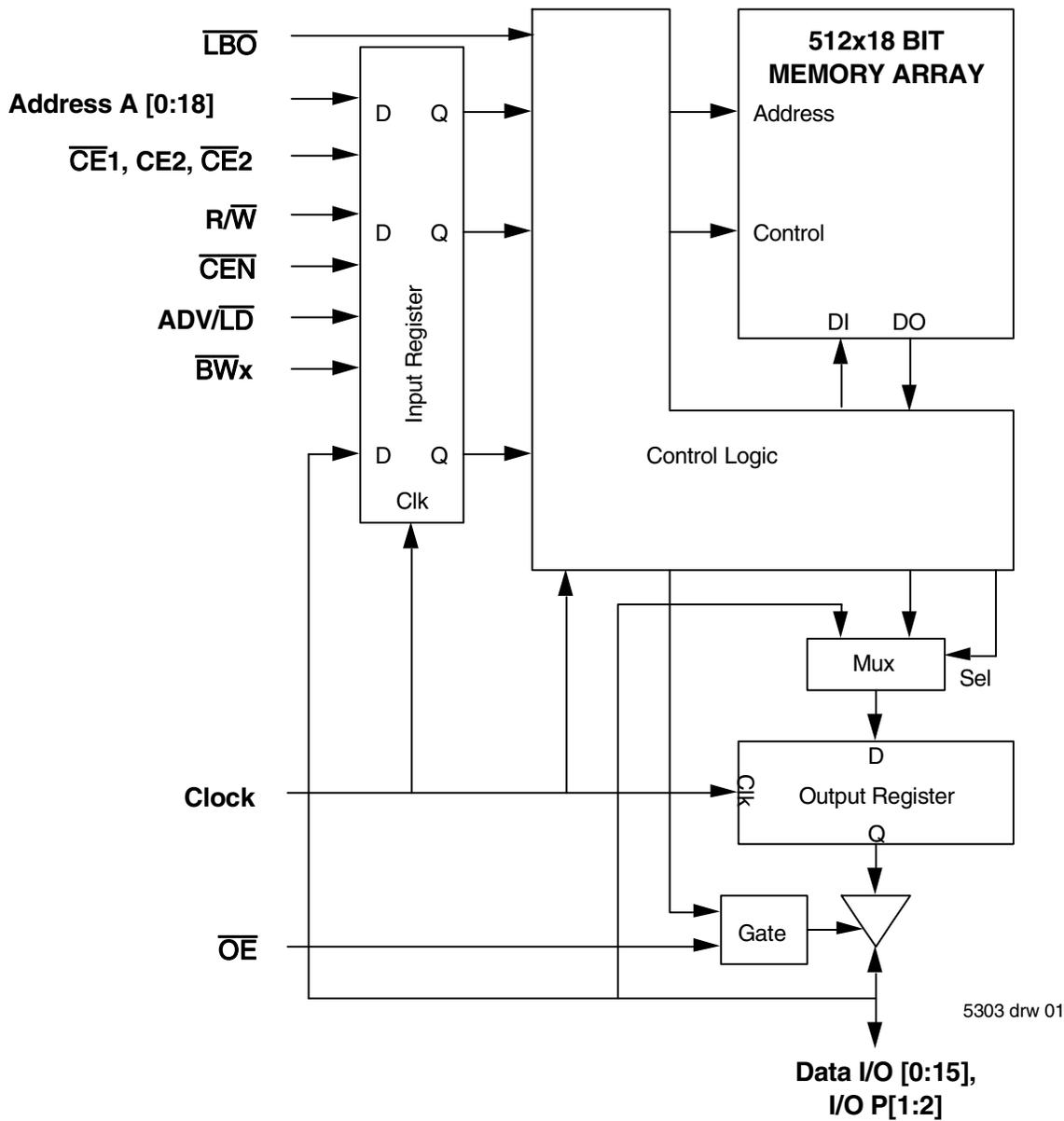
NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Functional Block Diagram



Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|---------------------|------|-----------------------|------|
| V _{DD} | Core Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{DDQ} | I/O Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| V _{SS} | Supply Voltage | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage - Inputs | 1.7 | — | V _{DD} +0.3 | V |
| V _{IH} | Input High Voltage - I/O | 1.7 | — | V _{DDQ} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽¹⁾ | — | 0.7 | V |

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NOTES:

- V_{IL} (min.) = -1.0V for pulse width less than tcvc/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

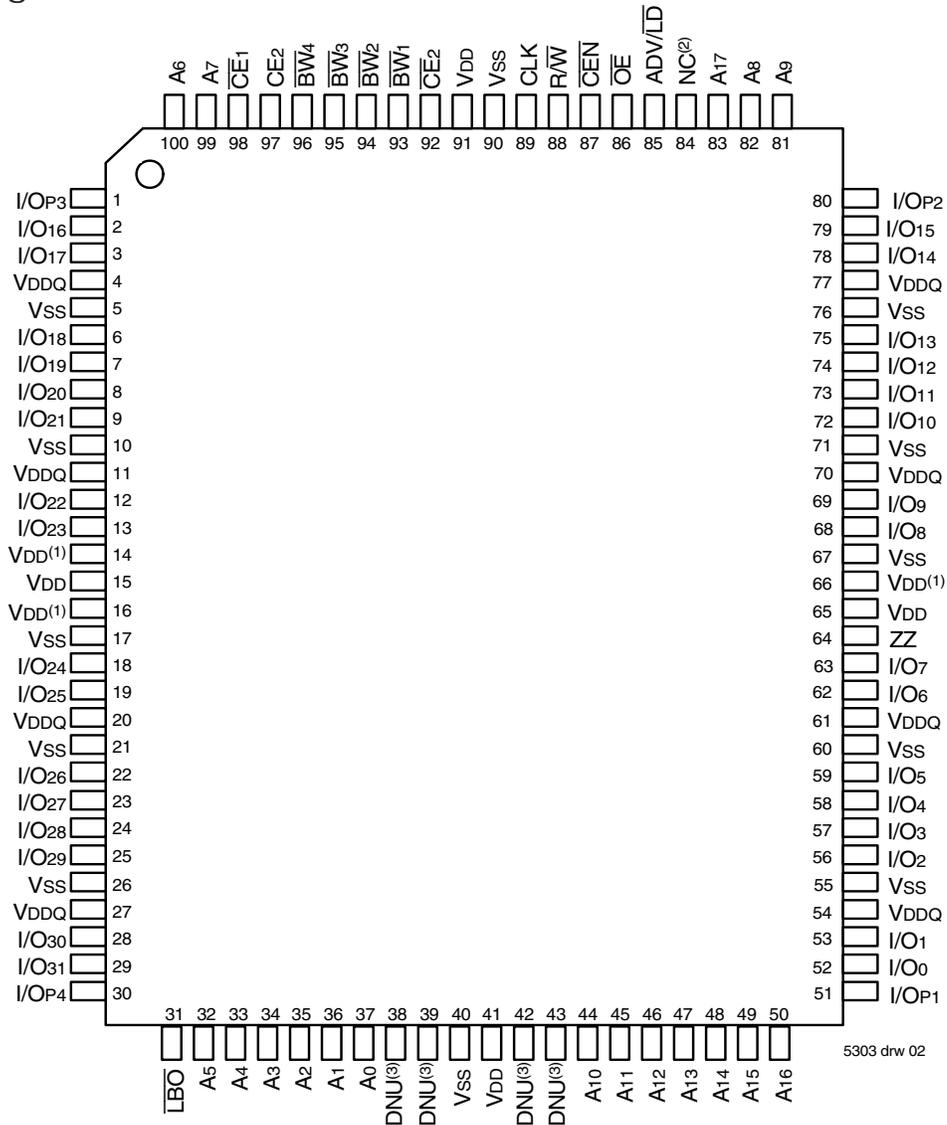
| Grade | Ambient Temperature ⁽¹⁾ | V _{SS} | V _{DD} | V _{DDQ} |
|------------|------------------------------------|-----------------|-----------------|------------------|
| Commercial | 0° C to +70° C | 0V | 3.3V±5% | 2.5V±5% |
| Industrial | -40° C to +85° C | 0V | 3.3V±5% | 2.5V±5% |

NOTES:

5303tbl 05

1. During production testing, the case temperature equals the ambient temperature.

Pin Configuration - 256K x 36

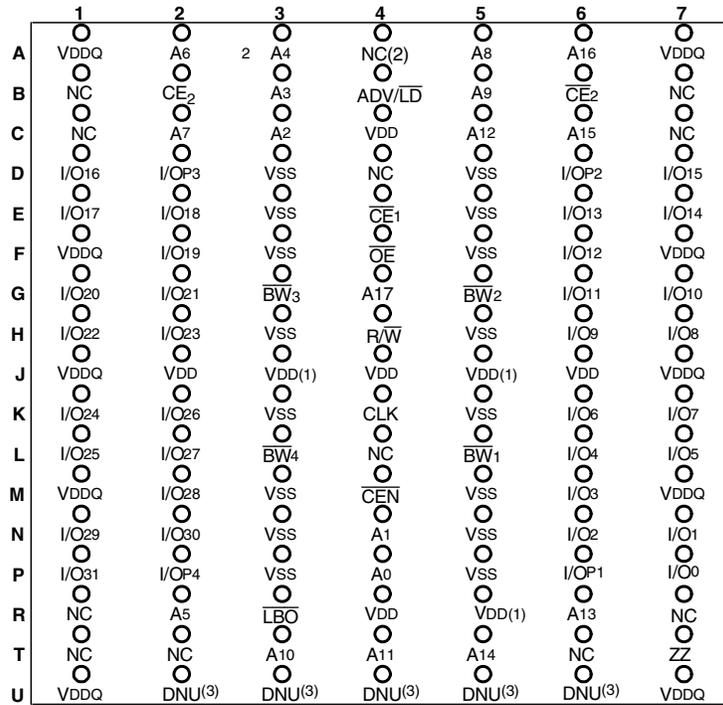


Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied Low (V_{SS}) or tied High (V_{DD}).

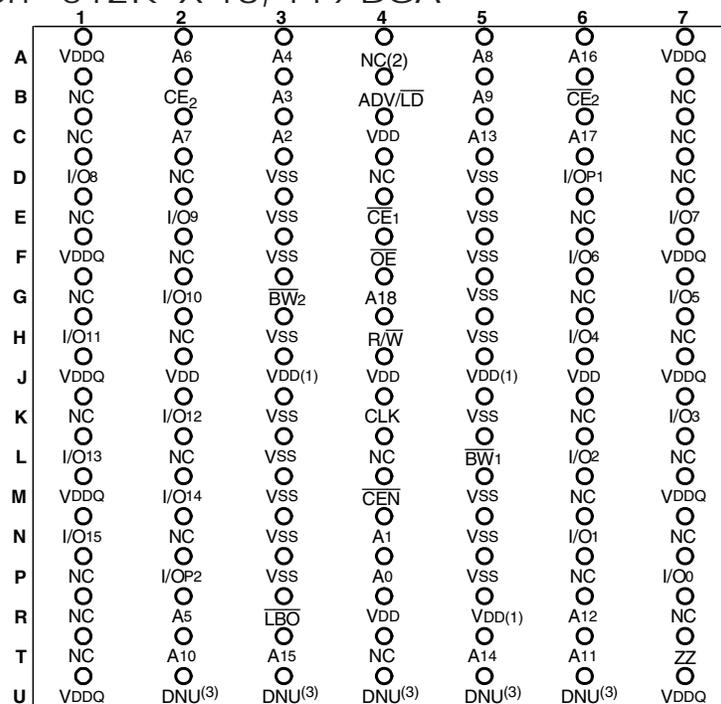
Pin Configuration - 256K X 36, 119 BGA



5303 drw 13A

Top View

Pin Configuration - 512K X 18, 119 BGA



5303 drw 13B

Top View

NOTES:

- J3, J5, and R5 do not have to be directly connected to VDD as long as the input voltage is $\geq V_{IH}$.
- A4 is reserved for future 16M.
- DNU = Do not use. Pin U2, U3, U4, U5 and U6 are reserved for respective JTAG pins: TMS, TDI, TCK, TDO and \overline{TRST} . The current die revision allows these pins to be left unconnected, tied LOW (Vss), or tied HIGH (Vdd).

Pin Configuration - 256K X 36, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|--------------------|-------------------|-------------------|--------------------|-------------------|--------------------|----------------------|-------------------|-------|-------------------|
| A | NC ⁽²⁾ | A7 | \overline{CE}_1 | \overline{BW}_3 | \overline{BW}_2 | \overline{CE}_2 | \overline{CEN} | ADV/ \overline{LD} | A17 | A8 | NC |
| B | NC | A6 | CE2 | \overline{BW}_4 | \overline{BW}_1 | CLK | R \overline{W} | \overline{OE} | NC ⁽²⁾ | A9 | NC ⁽²⁾ |
| C | I/OP3 | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/OP2 |
| D | I/O17 | I/O16 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O15 | I/O14 |
| E | I/O19 | I/O18 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O13 | I/O12 |
| F | I/O21 | I/O20 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O11 | I/O10 |
| G | I/O ₂₃ | I/O22 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O9 | I/O8 |
| H | VDD ⁽¹⁾ | VDD ⁽¹⁾ | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ |
| J | I/O25 | I/O24 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O7 | I/O6 |
| K | I/O27 | I/O26 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O5 | I/O4 |
| L | I/O29 | I/O28 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O3 | I/O2 |
| M | I/O31 | I/O30 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O1 | I/O0 |
| N | I/OP4 | NC | VDDQ | VSS | DNU ⁽³⁾ | NC | VDD ⁽¹⁾ | VSS | VDDQ | NC | I/OP1 |
| P | NC | NC ⁽²⁾ | A5 | A2 | DNU ⁽³⁾ | A1 | DNU ⁽³⁾ | A10 | A13 | A14 | NC |
| R | \overline{LBO} | NC ⁽²⁾ | A4 | A3 | DNU ⁽³⁾ | A0 | DNU ⁽³⁾ | A11 | A12 | A15 | A16 |

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Pin Configuration - 512K X 18, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|--------------------|-------------------|-------------------|--------------------|-------------------|--------------------|----------------------|-------------------|------|-------------------|
| A | NC ⁽²⁾ | A7 | \overline{CE}_1 | \overline{BW}_2 | NC | \overline{CE}_2 | \overline{CEN} | ADV/ \overline{LD} | A18 | A8 | A10 |
| B | NC | A6 | CE2 | NC | \overline{BW}_1 | CLK | R \overline{W} | \overline{OE} | NC ⁽²⁾ | A9 | NC ⁽²⁾ |
| C | NC | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/OP1 |
| D | NC | I/O8 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O7 |
| E | NC | I/O9 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O6 |
| F | NC | I/O10 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O5 |
| G | NC | I/O11 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O4 |
| H | VDD ⁽¹⁾ | VDD ⁽¹⁾ | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ |
| J | I/O12 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O3 | NC |
| K | I/O13 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O2 | NC |
| L | I/O14 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O1 | NC |
| M | I/O15 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O0 | NC |
| N | I/OP2 | NC | VDDQ | VSS | DNU ⁽³⁾ | NC | VDD ⁽¹⁾ | VSS | VDDQ | NC | NC |
| P | NC | NC ⁽²⁾ | A5 | A2 | DNU ⁽³⁾ | A1 | DNU ⁽³⁾ | A11 | A14 | A15 | NC |
| R | \overline{LBO} | NC ⁽²⁾ | A4 | A3 | DNU ⁽³⁾ | A0 | DNU ⁽³⁾ | A12 | A13 | A16 | A17 |

5303 tbl 25b

NOTES:

- H1, H2, and N7 do not have to be directly connected to VDD as long as the input voltage is $\geq V_{IH}$.
- B9, B11, A1, R2 and P2 is reserved for future 18M, 36M, 72M, 144M and 288M, respectively.
- DNU=Do not use. Pins P5, R5, P7, R7 and N5 are reserved for respective JTAG pins: TDI, TMS, TDO, TCK and \overline{TRST} on future revisions. The current die revision allows these pins to be left unconnected, tied LOW (Vss), or tied HIGH (VDD).

Synchronous Truth Table⁽¹⁾

| \overline{CEN} | R/ \overline{W} | Chip ⁽⁵⁾ Enable | ADV/ \overline{LD} | \overline{BW}_x | ADDRESS USED | PREVIOUS CYCLE | CURRENT CYCLE | I/O (2 cycles later) |
|------------------|-------------------|-------------------------------|----------------------|-------------------|-----------------|-----------------------------|---|-------------------------|
| L | L | Select | L | Valid | External | X | LOAD WRITE | D ⁽⁷⁾ |
| L | H | Select | L | X | External | X | LOAD READ | Q ⁽⁷⁾ |
| L | X | X | H | Valid | Internal | LOAD WRITE / BURST WRITE | BURST WRITE (Advance burst counter) ⁽²⁾ | D ⁽⁷⁾ |
| L | X | X | H | X | Internal | LOAD READ / BURST READ | BURST READ (Advance burst counter) ⁽²⁾ | Q ⁽⁷⁾ |
| L | X | Deselect | L | X | X | X | DESELECT or STOP ⁽³⁾ | HiZ |
| L | X | X | H | X | X | DESELECT / NOOP | NOOP | HiZ |
| H | X | X | X | X | X | X | SUSPEND ⁽⁴⁾ | Previous Value |

5303 tbl 08

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- When ADV/ \overline{LD} signal is sampled high, the internal burst counter is incremented. The R/ \overline{W} signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/ \overline{W} signal when the first address is loaded at the beginning of the burst cycle.
- Deselect cycle is initiated when either (\overline{CE}_1 , or \overline{CE}_2 is sampled high or \overline{CE}_2 is sampled low) and ADV/ \overline{LD} is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
- When \overline{CEN} is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- To select the chip requires $\overline{CE}_1 = L$, $\overline{CE}_2 = L$, $CE_2 = H$ on these chip enables. Chip is deselected if any one of the chip enables is false.
- Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
- Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes⁽¹⁾

| OPERATION | R/ \overline{W} | \overline{BW}_1 | \overline{BW}_2 | \overline{BW}_3 ⁽³⁾ | \overline{BW}_4 ⁽³⁾ |
|---|-------------------|-------------------|-------------------|----------------------------------|----------------------------------|
| READ | H | X | X | X | X |
| WRITE ALL BYTES | L | L | L | L | L |
| WRITE BYTE 1 (I/O[0:7], I/Op1) ⁽²⁾ | L | L | H | H | H |
| WRITE BYTE 2 (I/O[8:15], I/Op2) ⁽²⁾ | L | H | L | H | H |
| WRITE BYTE 3 (I/O[16:23], I/Op3) ^(2,3) | L | H | H | L | H |
| WRITE BYTE 4 (I/O[24:31], I/Op4) ^(2,3) | L | H | H | H | L |
| NO WRITE | L | H | H | H | H |

5303 tbl 09

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- Multiple bytes may be selected during the same cycle.
- N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{\text{LBO}} = \text{VDD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

5303 tbl 10

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table ($\overline{\text{LBO}} = \text{Vss}$)

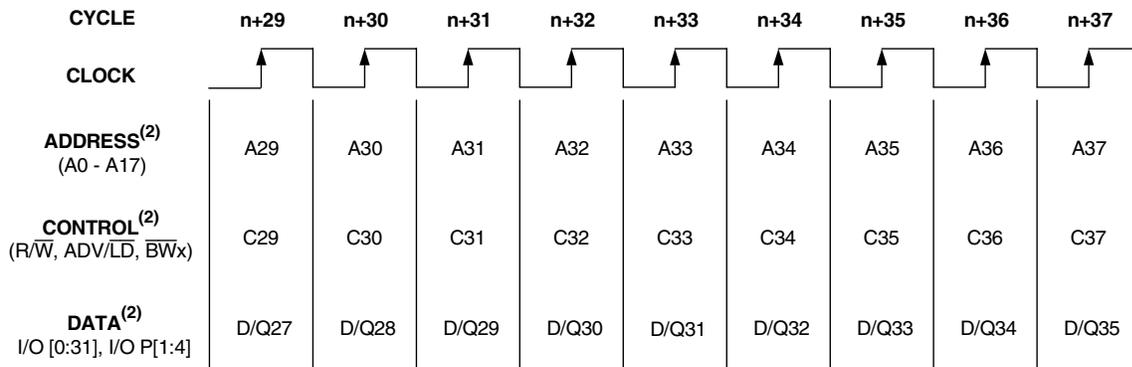
| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5303 tbl 11

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram⁽¹⁾



5303 drw 03

NOTES:

1. This assumes $\overline{\text{CEN}}$, $\overline{\text{CE1}}$, CE2 , $\overline{\text{CE2}}$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles⁽²⁾

| Cycle | Address | R/W | ADV/LD | $\overline{CE}^{(1)}$ | \overline{CEN} | \overline{BW}_x | \overline{OE} | I/O | Comments |
|-------|----------------|-----|--------|-----------------------|------------------|-------------------|-----------------|------------------|------------------|
| n | A ₀ | H | L | L | L | X | X | X | Load read |
| n+1 | X | X | H | X | L | X | X | X | Burst read |
| n+2 | A ₁ | H | L | L | L | X | L | Q ₀ | Load read |
| n+3 | X | X | L | H | L | X | L | Q ₀₊₁ | Deselect or STOP |
| n+4 | X | X | H | X | L | X | L | Q ₁ | NOOP |
| n+5 | A ₂ | H | L | L | L | X | X | Z | Load read |
| n+6 | X | X | H | X | L | X | X | Z | Burst read |
| n+7 | X | X | L | H | L | X | L | Q ₂ | Deselect or STOP |
| n+8 | A ₃ | L | L | L | L | L | L | Q ₂₊₁ | Load write |
| n+9 | X | X | H | X | L | L | X | Z | Burst write |
| n+10 | A ₄ | L | L | L | L | L | X | D ₃ | Load write |
| n+11 | X | X | L | H | L | X | X | D ₃₊₁ | Deselect or STOP |
| n+12 | X | X | H | X | L | X | X | D ₄ | NOOP |
| n+13 | A ₅ | L | L | L | L | L | X | Z | Load write |
| n+14 | A ₆ | H | L | L | L | X | X | Z | Load read |
| n+15 | A ₇ | L | L | L | L | L | X | D ₅ | Load write |
| n+16 | X | X | H | X | L | L | L | Q ₆ | Burst write |
| n+17 | A ₈ | H | L | L | L | X | X | D ₇ | Load read |
| n+18 | X | X | H | X | L | X | X | D ₇₊₁ | Burst read |
| n+19 | A ₉ | L | L | L | L | L | L | Q ₈ | Load write |

5303 tbl 12

NOTES:

- $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.
- H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation⁽¹⁾

| Cycle | Address | R/W | ADV/LD | $\overline{CE}^{(2)}$ | \overline{CEN} | \overline{BW}_x | \overline{OE} | I/O | Comments |
|-------|----------------|-----|--------|-----------------------|------------------|-------------------|-----------------|----------------|---|
| n | A ₀ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | L | X | X | X | Clock Setup Valid |
| n+2 | X | X | X | X | X | X | L | Q ₀ | Contents of Address A ₀ Read Out |

5303 tbl 13

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.

Burst Read Operation⁽¹⁾

| Cycle | Address | R/ \bar{W} | ADV/ \bar{LD} | $\bar{CE}^{(2)}$ | \bar{CEN} | \bar{BW}_x | \bar{OE} | I/O | Comments |
|-------|----------------|--------------|-----------------|------------------|-------------|--------------|------------|------------------|--|
| n | A ₀ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | X | X | X | Clock Setup Valid, Advance Counter |
| n+2 | X | X | H | X | L | X | L | Q ₀ | Address A ₀ Read Out, Inc. Count |
| n+3 | X | X | H | X | L | X | L | Q ₀₊₁ | Address A ₀₊₁ Read Out, Inc. Count |
| n+4 | X | X | H | X | L | X | L | Q ₀₊₂ | Address A ₀₊₂ Read Out, Inc. Count |
| n+5 | A ₁ | H | L | L | L | X | L | Q ₀₊₃ | Address A ₀₊₃ Read Out, Load A ₁ |
| n+6 | X | X | H | X | L | X | L | Q ₀ | Address A ₀ Read Out, Inc. Count |
| n+7 | X | X | H | X | L | X | L | Q ₁ | Address A ₁ Read Out, Inc. Count |
| n+8 | A ₂ | H | L | L | L | X | L | Q ₁₊₁ | Address A ₁₊₁ Read Out, Load A ₂ |

5303 tbl 14

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Write Operation⁽¹⁾

| Cycle | Address | R/ \bar{W} | ADV/ \bar{LD} | $\bar{CE}^{(2)}$ | \bar{CEN} | \bar{BW}_x | \bar{OE} | I/O | Comments |
|-------|----------------|--------------|-----------------|------------------|-------------|--------------|------------|----------------|---------------------------------|
| n | A ₀ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | L | X | X | X | Clock Setup Valid |
| n+2 | X | X | X | X | L | X | X | D ₀ | Write to Address A ₀ |

5303 tbl 15

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Burst Write Operation⁽¹⁾

| Cycle | Address | R/ \bar{W} | ADV/ \bar{LD} | $\bar{CE}^{(2)}$ | \bar{CEN} | \bar{BW}_x | \bar{OE} | I/O | Comments |
|-------|----------------|--------------|-----------------|------------------|-------------|--------------|------------|------------------|---|
| n | A ₀ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | L | X | X | Clock Setup Valid, Inc. Count |
| n+2 | X | X | H | X | L | L | X | D ₀ | Address A ₀ Write, Inc. Count |
| n+3 | X | X | H | X | L | L | X | D ₀₊₁ | Address A ₀₊₁ Write, Inc. Count |
| n+4 | X | X | H | X | L | L | X | D ₀₊₂ | Address A ₀₊₂ Write, Inc. Count |
| n+5 | A ₁ | L | L | L | L | L | X | D ₀₊₃ | Address A ₀₊₃ Write, Load A ₁ |
| n+6 | X | X | H | X | L | L | X | D ₀ | Address A ₀ Write, Inc. Count |
| n+7 | X | X | H | X | L | L | X | D ₁ | Address A ₁ Write, Inc. Count |
| n+8 | A ₂ | L | L | L | L | L | X | D ₁₊₁ | Address A ₁₊₁ Write, Load A ₂ |

5303 tbl 16

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Read Operation with Clock Enable Used⁽¹⁾

| Cycle | Address | R/ \bar{W} | ADV/ \bar{LD} | $\bar{CE}^{(2)}$ | \bar{CEN} | \bar{BW}_x | \bar{OE} | I/O | Comments |
|-------|----------------|--------------|-----------------|------------------|-------------|--------------|------------|----------------|---|
| n | A ₀ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored |
| n+2 | A ₁ | H | L | L | L | X | X | X | Clock Valid |
| n+3 | X | X | X | X | H | X | L | Q ₀ | Clock Ignored, Data Q ₀ is on the bus. |
| n+4 | X | X | X | X | H | X | L | Q ₀ | Clock Ignored, Data Q ₀ is on the bus. |
| n+5 | A ₂ | H | L | L | L | X | L | Q ₀ | Address A ₀ Read out (bus trans.) |
| n+6 | A ₃ | H | L | L | L | X | L | Q ₁ | Address A ₁ Read out (bus trans.) |
| n+7 | A ₄ | H | L | L | L | X | L | Q ₂ | Address A ₂ Read out (bus trans.) |

5303 tbl 17

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Write Operation with Clock Enable Used⁽¹⁾

| Cycle | Address | R/ \bar{W} | ADV/ \bar{LD} | $\bar{CE}^{(2)}$ | \bar{CEN} | \bar{BW}_x | \bar{OE} | I/O | Comments |
|-------|----------------|--------------|-----------------|------------------|-------------|--------------|------------|----------------|---------------------------------|
| n | A ₀ | L | L | L | L | L | X | X | Address and Control meet setup. |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored. |
| n+2 | A ₁ | L | L | L | L | L | X | X | Clock Valid. |
| n+3 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+4 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+5 | A ₂ | L | L | L | L | L | X | D ₀ | Write Data D ₀ |
| n+6 | A ₃ | L | L | L | L | L | X | D ₁ | Write Data D ₁ |
| n+7 | A ₄ | L | L | L | L | L | X | D ₂ | Write Data D ₂ |

5303 tbl 18

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Read Operation with Chip Enable Used⁽¹⁾

| Cycle | Address | R/ \overline{W} | ADV/ \overline{LD} | $\overline{CE}^{(2)}$ | \overline{CEN} | \overline{BW}_x | \overline{OE} | I/O ⁽³⁾ | Comments |
|-------|----------------|-------------------|----------------------|-----------------------|------------------|-------------------|-----------------|--------------------|--|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | ? | Deselected. |
| n+2 | A ₀ | H | L | L | L | X | X | Z | Address and Control meet setup |
| n+3 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+4 | A ₁ | H | L | L | L | X | L | Q ₀ | Address A ₀ Read out. Load A ₁ . |
| n+5 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+6 | X | X | L | H | L | X | L | Q ₁ | Address A ₁ Read out. Deselected. |
| n+7 | A ₂ | H | L | L | L | X | X | Z | Address and control meet setup. |
| n+8 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+9 | X | X | L | H | L | X | L | Q ₂ | Address A ₂ Read out. Deselected. |

5303 tbl 19

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used⁽¹⁾

| Cycle | Address | R/ \overline{W} | ADV/ \overline{LD} | $\overline{CE}^{(2)}$ | \overline{CEN} | \overline{BW}_x | \overline{OE} | I/O ⁽³⁾ | Comments |
|-------|----------------|-------------------|----------------------|-----------------------|------------------|-------------------|-----------------|--------------------|--|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | ? | Deselected. |
| n+2 | A ₀ | L | L | L | L | L | X | Z | Address and Control meet setup |
| n+3 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+4 | A ₁ | L | L | L | L | L | X | D ₀ | Address D ₀ Write in. Load A ₁ . |
| n+5 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+6 | X | X | L | H | L | X | X | D ₁ | Address D ₁ Write in. Deselected. |
| n+7 | A ₂ | L | L | L | L | L | X | Z | Address and control meet setup. |
| n+8 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+9 | X | X | L | H | L | X | X | D ₂ | Address D ₂ Write in. Deselected. |

5303 tbl 20

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|------------|---|---|------|------|---------|
| $ I_{LI} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 5 | μA |
| $ I_{LI} $ | \overline{LBO} Input Leakage Current ⁽¹⁾ | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 30 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{OUT} = 0V \text{ to } V_{DDQ}, \text{ Device Deselected}$ | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +6mA, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -6mA, V_{DD} = \text{Min.}$ | 2.0 | — | V |

NOTE:

5303 tbl 21

1. The \overline{LBO} pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ ($V_{DD} = 3.3V \pm 5\%$)

| Symbol | Parameter | Test Conditions | 150MHz | | 133MHz | | 100MHz | | Unit |
|-----------|------------------------------------|--|--------|-----|--------|-----|--------|-----|------|
| | | | Com'l | Ind | Com'l | Ind | Com'l | Ind | |
| I_{DD} | Operating Power Supply Current | Device Selected, Outputs Open, $ADV/\overline{LD} = X, V_{DD} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$ | 325 | 345 | 300 | 320 | 250 | 270 | mA |
| I_{SB1} | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$ | 40 | 60 | 40 | 60 | 40 | 60 | mA |
| I_{SB2} | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 120 | 140 | 110 | 130 | 100 | 120 | mA |
| I_{SB3} | Idle Power Supply Current | Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}, V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 40 | 60 | 40 | 60 | 40 | 60 | mA |
| I_{ZZ} | Full Sleep Mode Supply Current | Device Selected, Outputs Open, $\overline{CEN} \leq V_{IL}, V_{DD} = \text{Max.}, ZZ \geq V_{HD}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 40 | 60 | 40 | 60 | 40 | 60 | mA |

NOTES:

5303 tbl 22

- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/tcyc; $f=0$ means no input lines are changing.
- For I/Os $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$.

AC Test Load

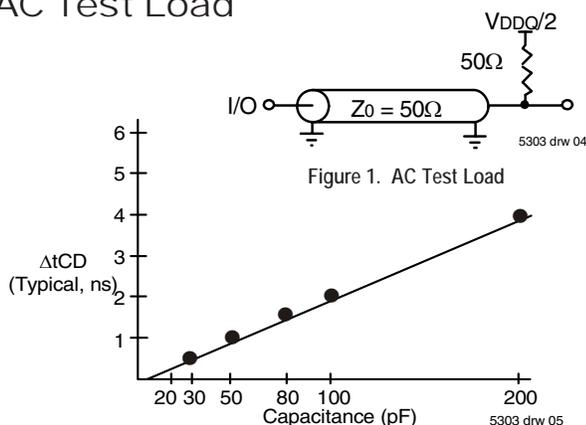


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions ($V_{DDQ} = 2.5V$)

| | |
|--------------------------------|--------------|
| Input Pulse Levels | 0 to 2.5V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | $V_{DDQ}/2$ |
| Output Timing Reference Levels | $V_{DDQ}/2$ |
| AC Test Load | See Figure 1 |

5303 tbl 23

AC Electrical Characteristics

(V_{DD} = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

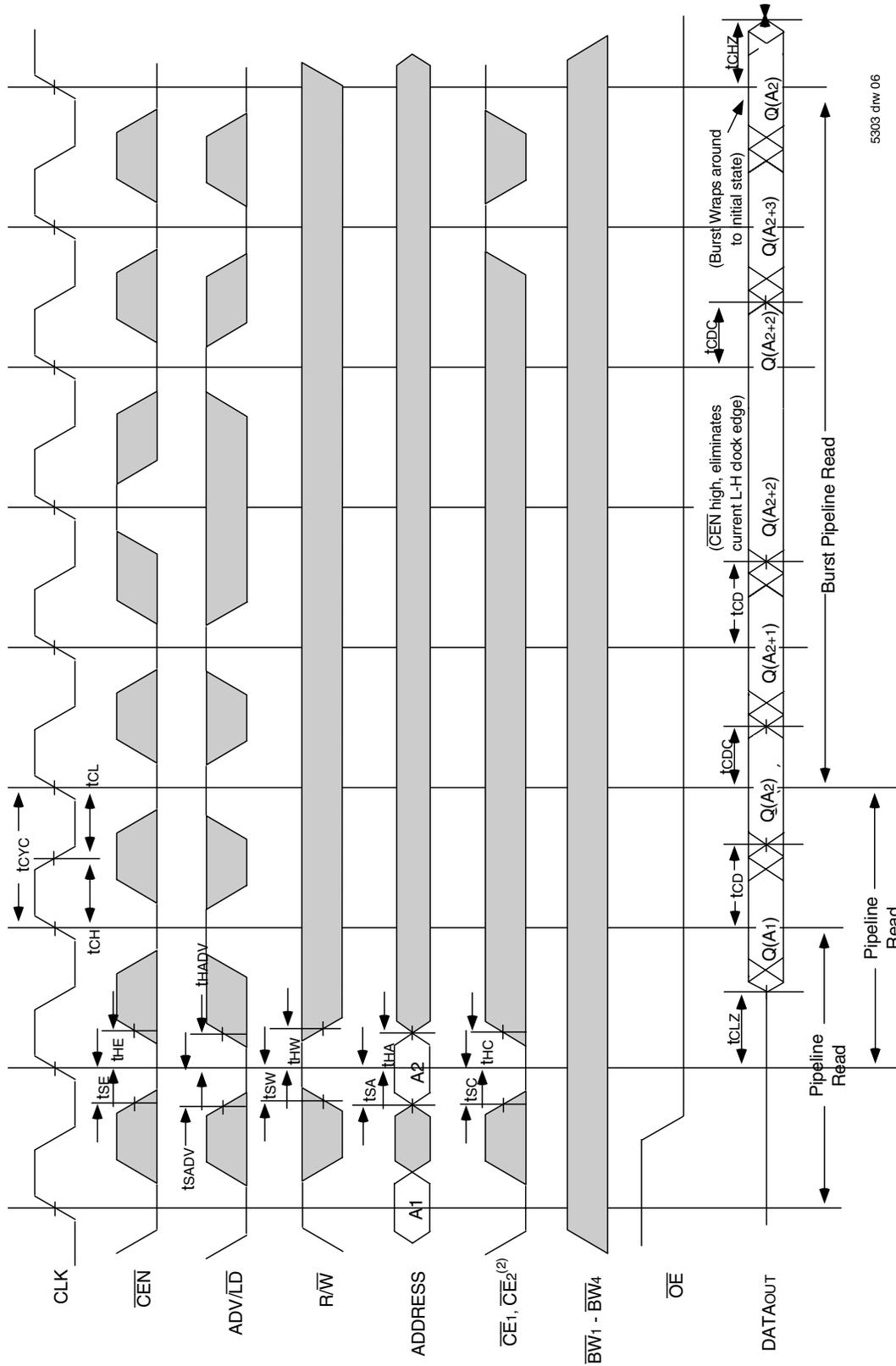
| Symbol | Parameter | 150MHz | | 133MHz | | 100MHz | | Unit |
|-------------------------------------|---|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CYC} | Clock Cycle Time | 6.7 | — | 7.5 | — | 10 | — | ns |
| t _F ⁽¹⁾ | Clock Frequency | — | 150 | — | 133 | — | 100 | MHz |
| t _{CH} ⁽²⁾ | Clock High Pulse Width | 2.0 | — | 2.2 | — | 3.2 | — | ns |
| t _{CL} ⁽²⁾ | Clock Low Pulse Width | 2.0 | — | 2.2 | — | 3.2 | — | ns |
| Output Parameters | | | | | | | | |
| t _{CD} | Clock High to Valid Data | — | 3.8 | — | 4.2 | — | 5 | ns |
| t _{CDc} | Clock High to Data Change | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{CLZ} ^(3,4,5) | Clock High to Output Active | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{CHZ} ^(3,4,5) | Clock High to Data High-Z | 1.5 | 3 | 1.5 | 3 | 1.5 | 3.3 | ns |
| t _{OE} | Output Enable Access Time | — | 3.8 | — | 4.2 | — | 5 | ns |
| t _{OLZ} ^(3,4) | Output Enable Low to Data Active | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ^(3,4) | Output Enable High to Data High-Z | — | 3.8 | — | 4.2 | — | 5 | ns |
| Set Up Times | | | | | | | | |
| t _{SE} | Clock Enable Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{SA} | Address Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{SD} | Data In Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{SW} | Read/Write (R/W) Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{ADV} | Advance/Load (ADV/LD) Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{SC} | Chip Enable/Select Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| t _{SB} | Byte Write Enable (B _W x) Setup Time | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| Hold Times | | | | | | | | |
| t _{HE} | Clock Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HA} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HD} | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HW} | Read/Write (R/W) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HADV} | Advance/Load (ADV/LD) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HC} | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HB} | Byte Write Enable (B _W x) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |

NOTES:

5303 tbl 24

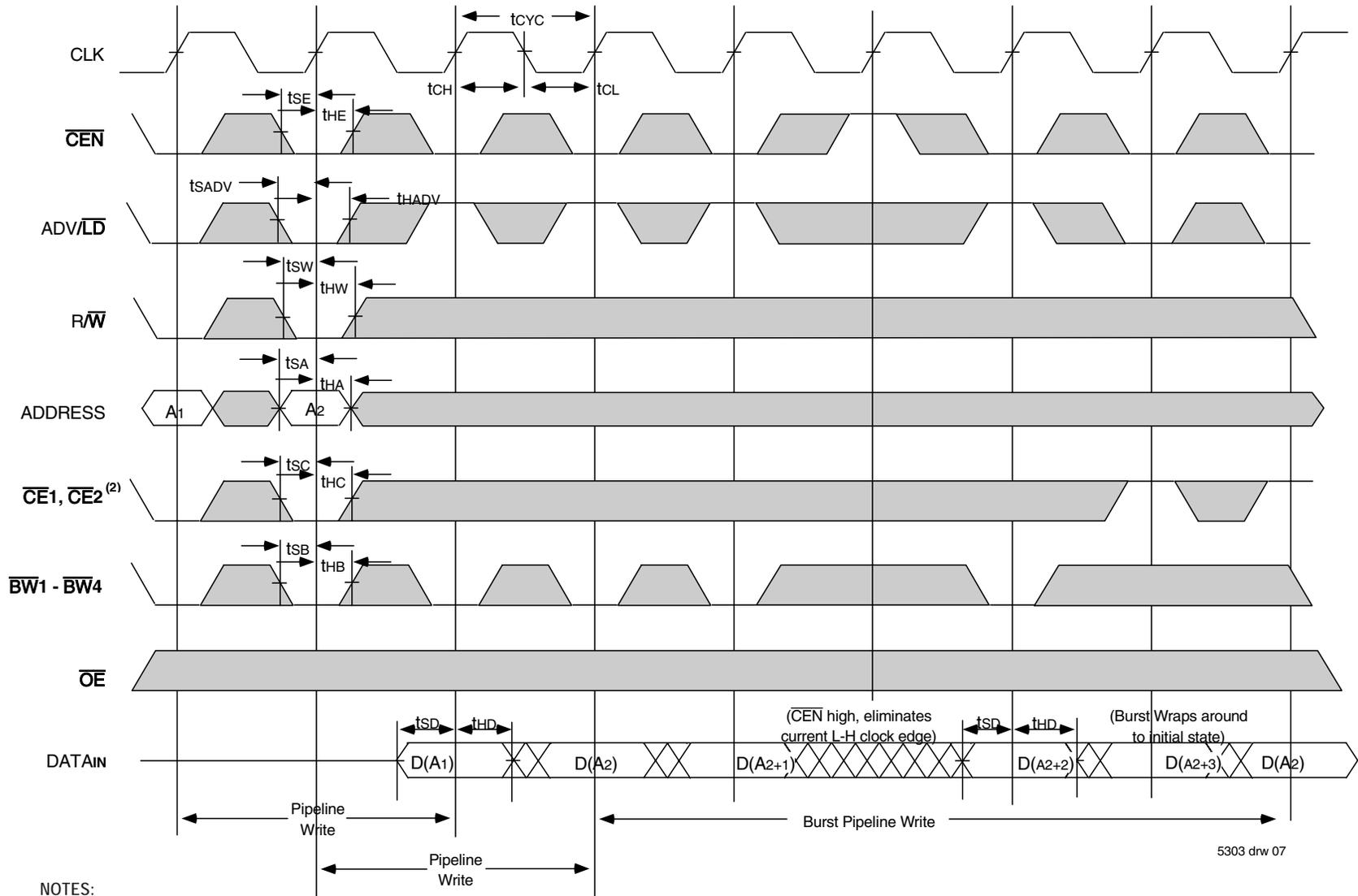
- t_F = 1/t_{CYC}.
- Measured as HIGH above 0.6V_{DD0} and LOW below 0.4V_{DD0}.
- Transition is measured ±200mV from steady-state.
- These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
- To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).

Timing Waveform of Read Cycle^(1,2,3,4)



NOTES:

1. $Q(A_1)$ represents the first output from the external address A_1 . $Q(A_2)$ represents the first output from the external address A_2 . $Q(A_{2+1})$ represents the next output data in the burst sequence of the base address A_2 , etc., where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input.
2. CE_2 timing transitions are identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals. For example, when \overline{CE}_1 and \overline{CE}_2 are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. $\overline{R/W}$ is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the $\overline{R/W}$ signal when new address and control are loaded into the SRAM.

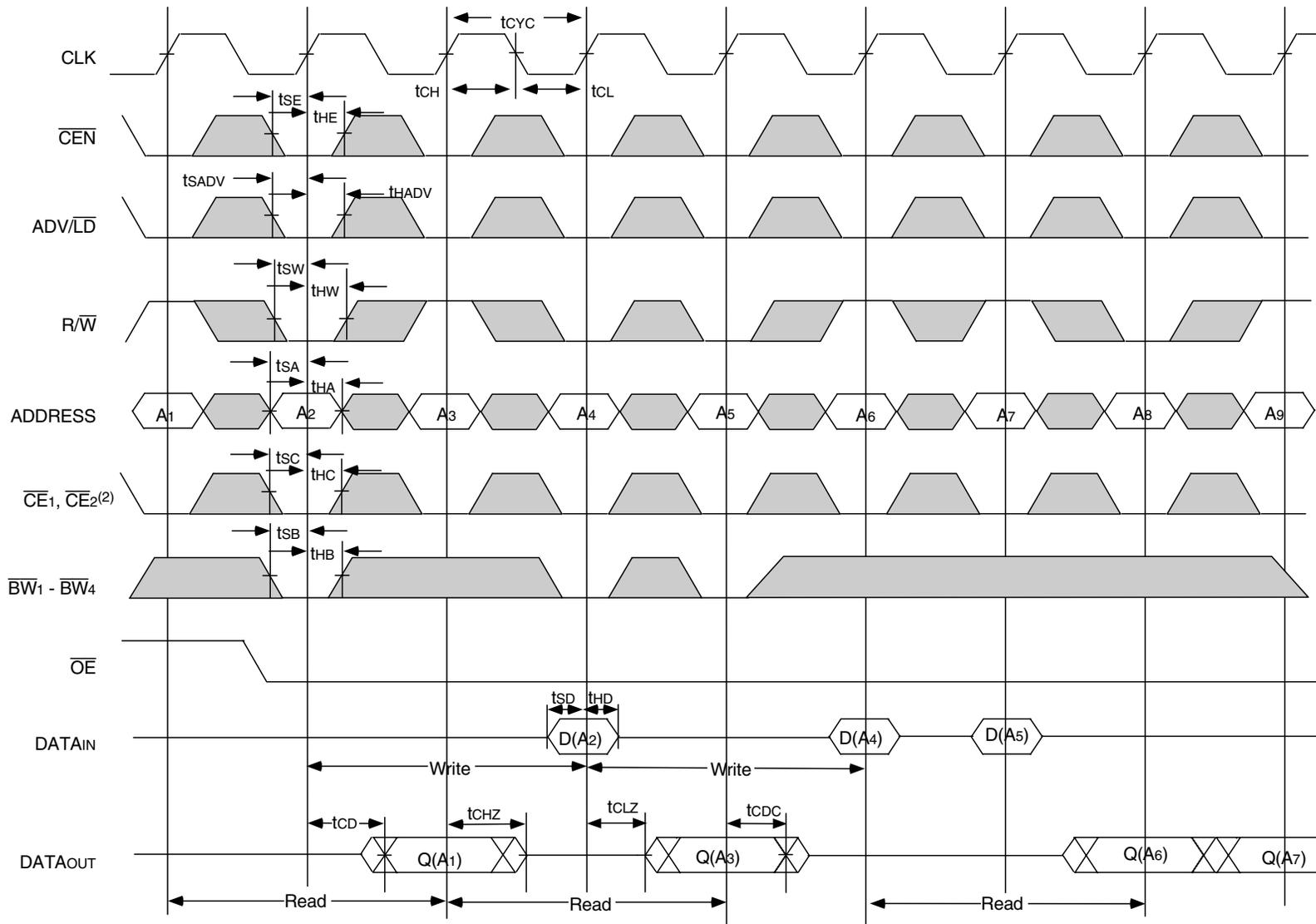


NOTES:

1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{\text{LB0}}$ input.
2. CE2 timing transitions are identical but inverted to the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ signals. For example, when $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. $\overline{\text{R/W}}$ is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the $\overline{\text{R/W}}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{\text{BWx}}$) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{R/W}}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Write Cycles (1,2,3,4,5)

Timing Waveform of Combined Read and Write Cycles (1,2,3)

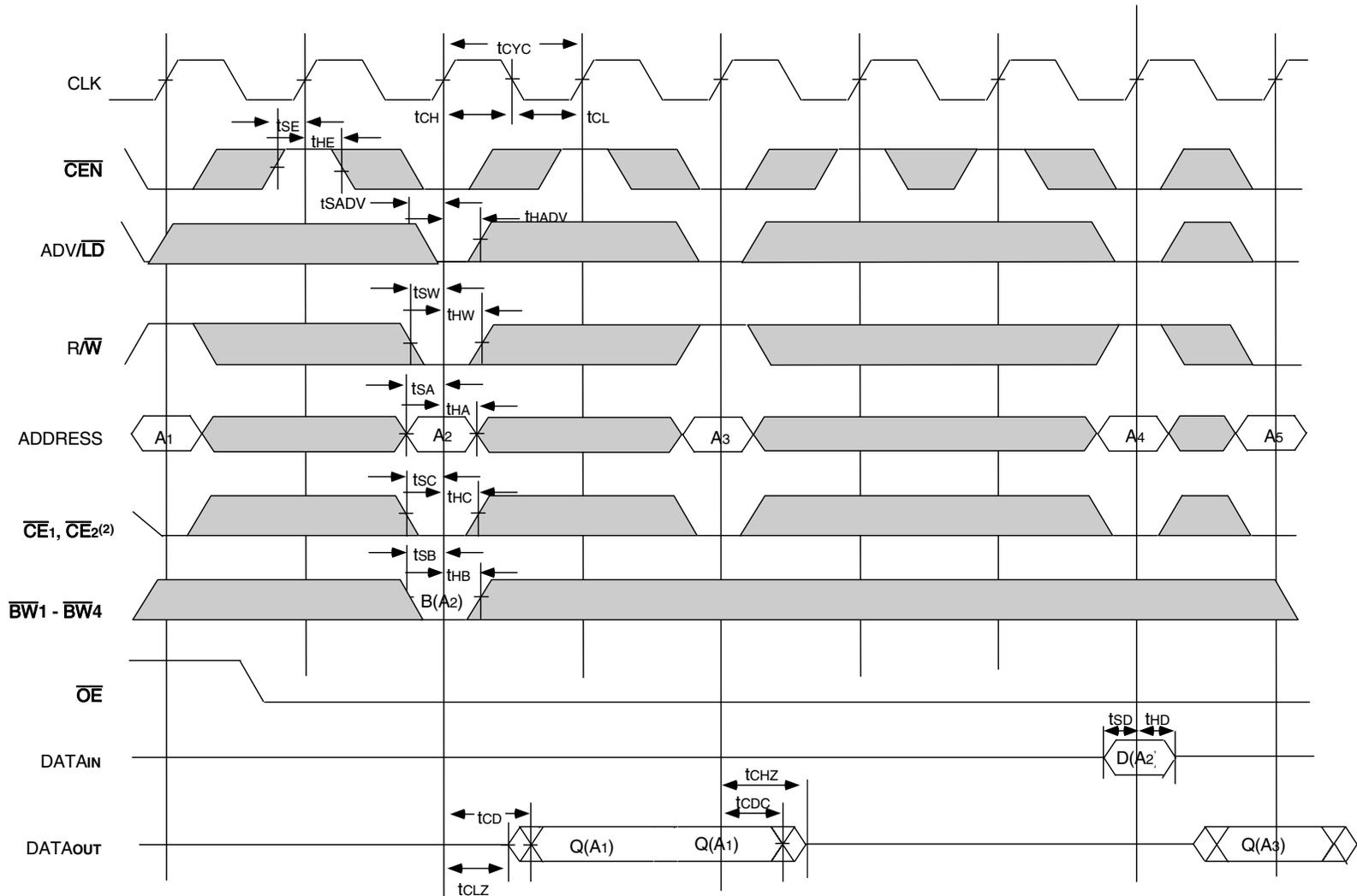


5303 drw 08

NOTES:

1. Q(A₁) represents the first output from the external address A₁. D(A₂) represents the input data to the SRAM corresponding to address A₂.
2. CE₂ timing transitions are identical but inverted to the CE₁ and CE₂ signals. For example, when CE₁ and CE₂ are LOW on this waveform, CE₂ is HIGH.
3. Individual Byte Write signals (\overline{BWx}) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of **CEN** Operation (1,2,3,4)

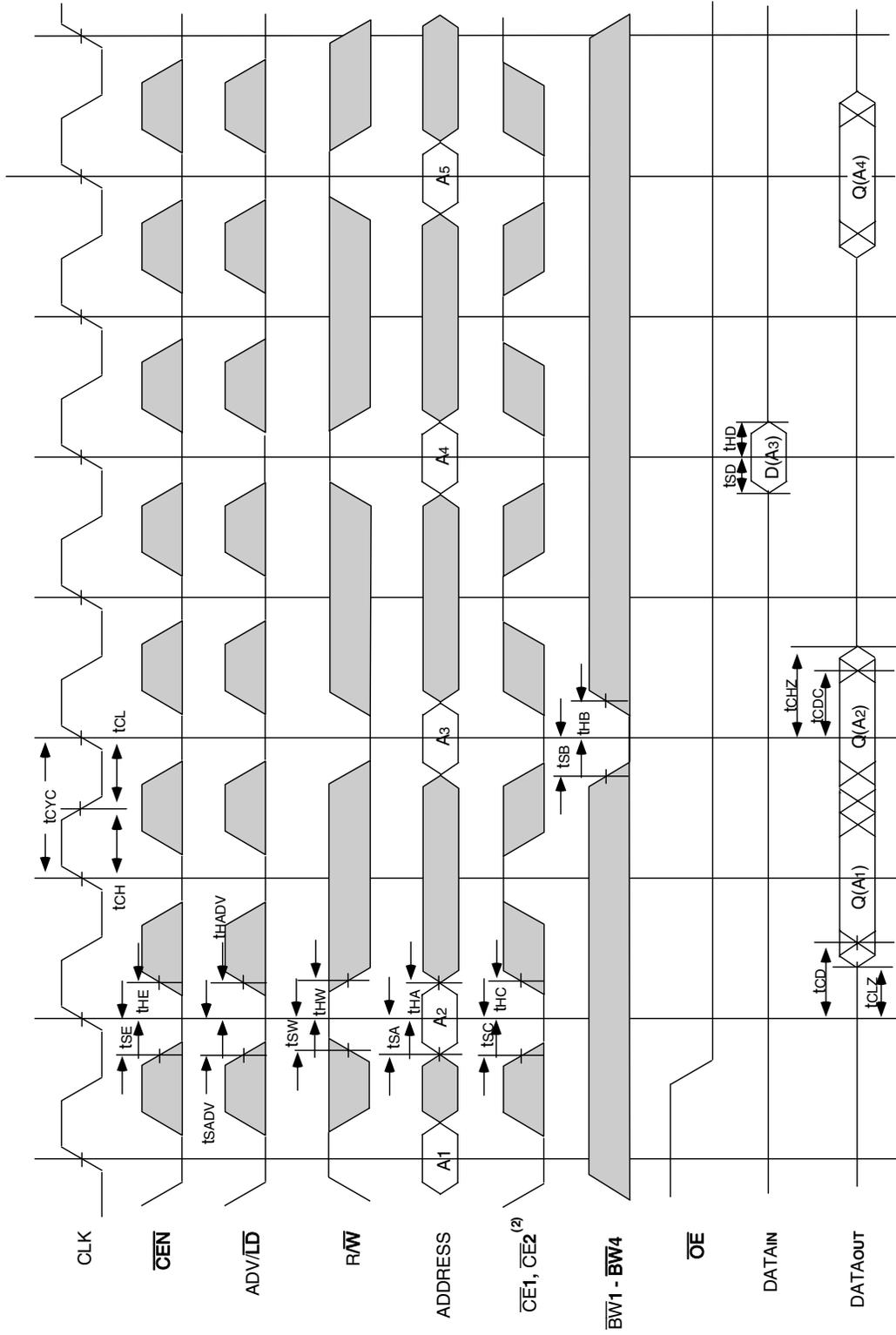


5303 drw 09

NOTES:

1. Q (A_i) represents the first output from the external address A₁. D (A₂) represents the input data to the SRAM corresponding to address A₂.
2. CE₂ timing transitions are identical but inverted to the CE₁ and CE₂ signals. For example, when CE₁ and CE₂ are LOW on this waveform, CE₂ is HIGH.
3. CEN when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (BW_x) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CS}}$ Operation^(1,2,3,4)

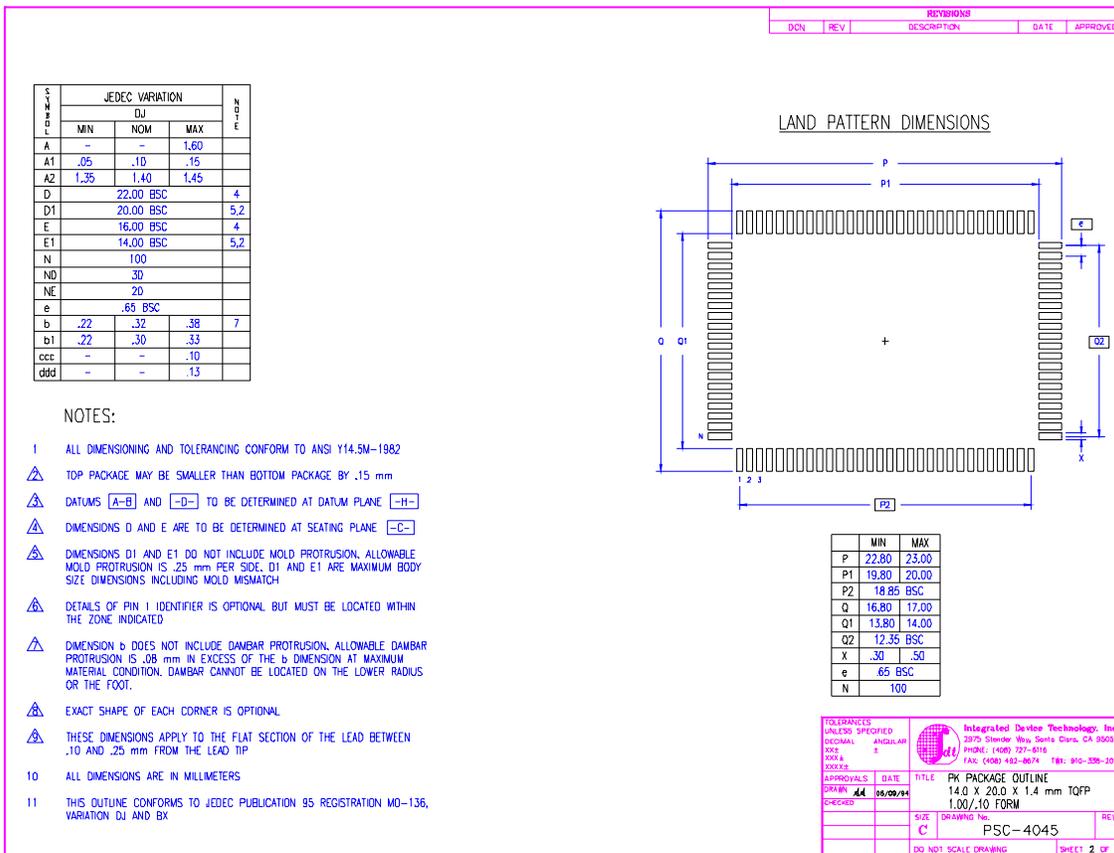
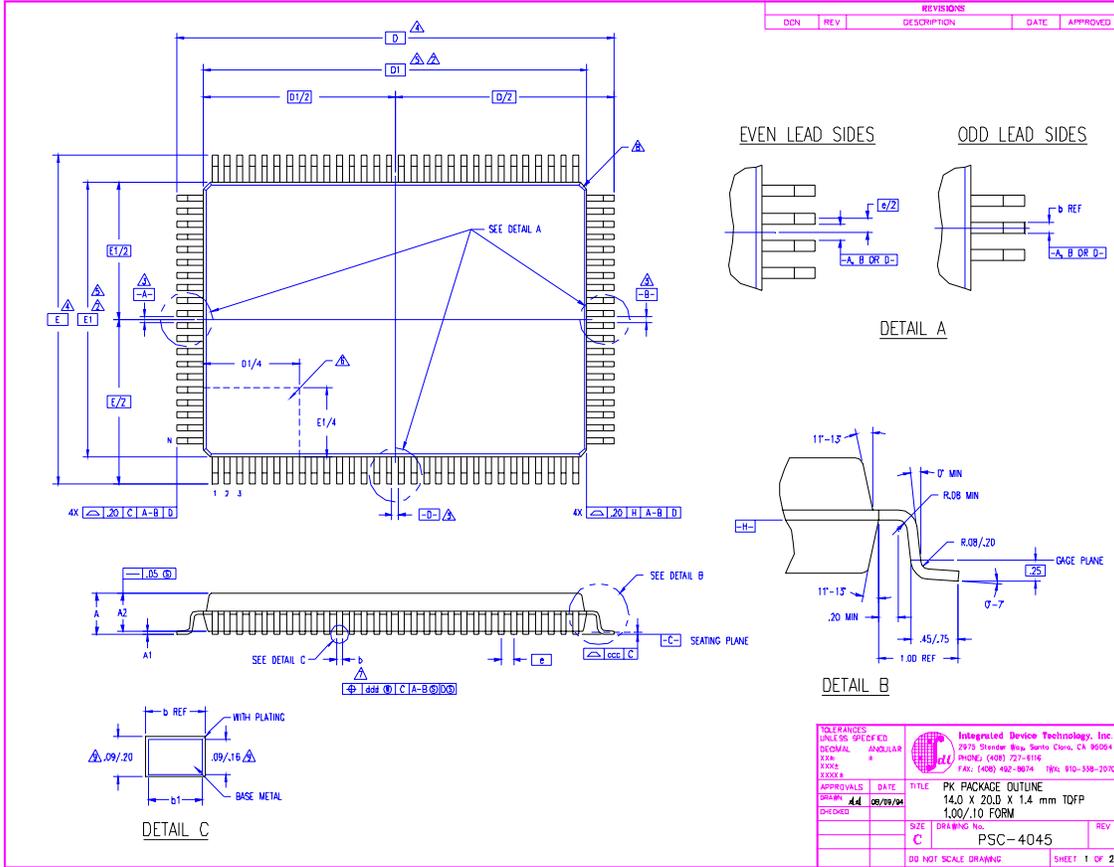


5303 drw 10

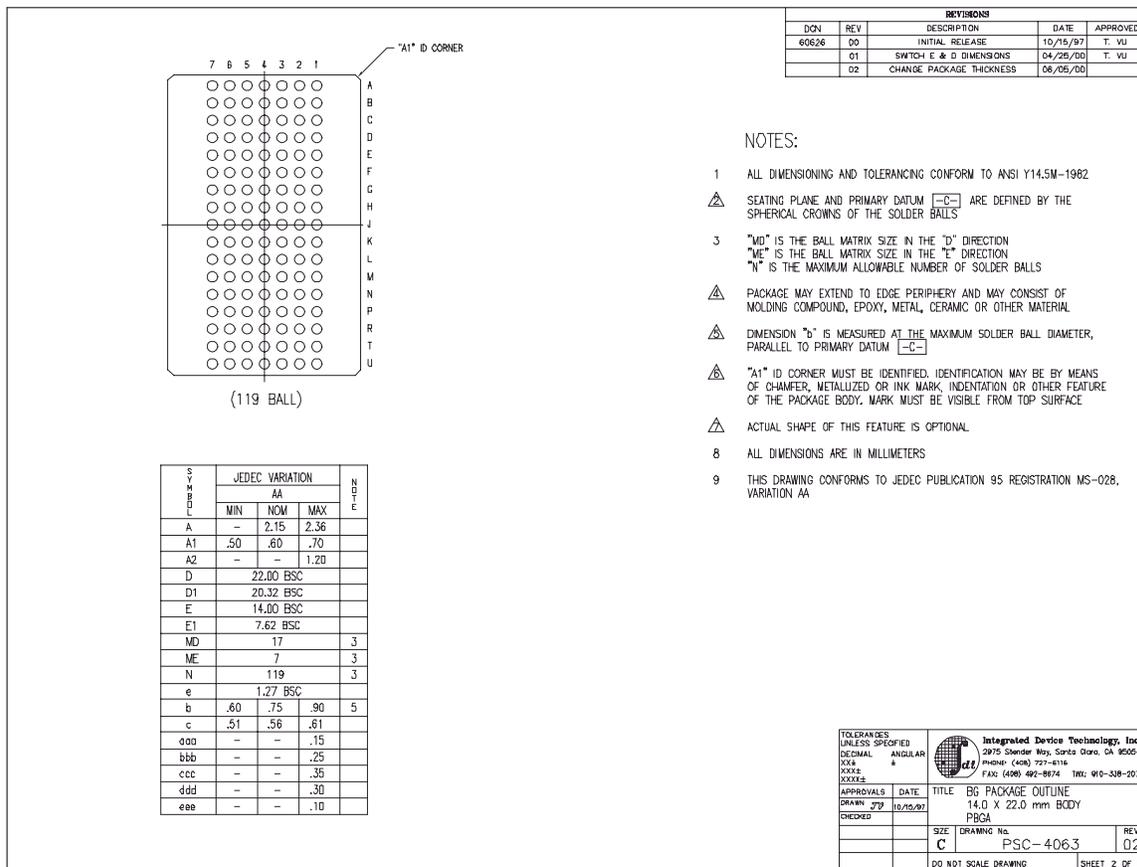
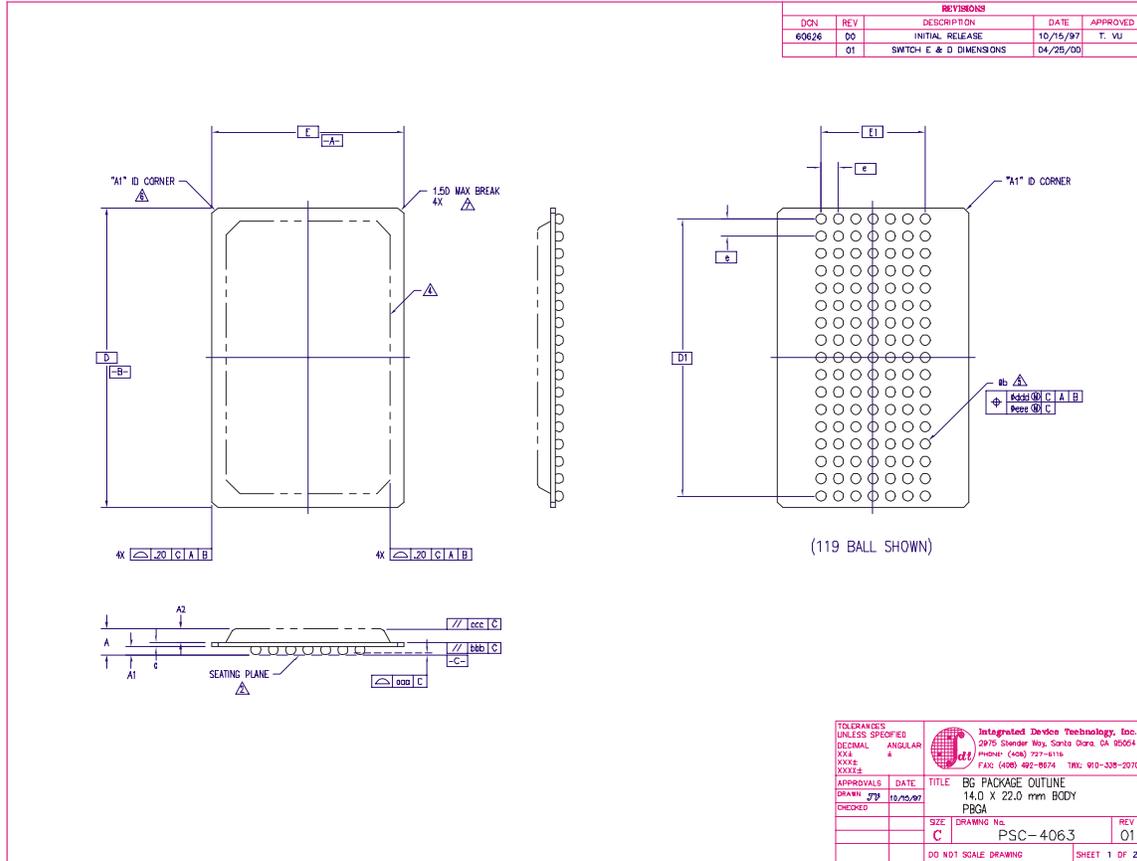
NOTES:

1. Q(A₁) represents the first output from the external address A₁. D(A₃) represents the input data to the SRAM corresponding to address A₃.
2. $\overline{\text{CE2}}$ timing transitions are identical but inverted to the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ signals. For example, when $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are LOW on this waveform, $\overline{\text{CE2}}$ is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{RW}}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

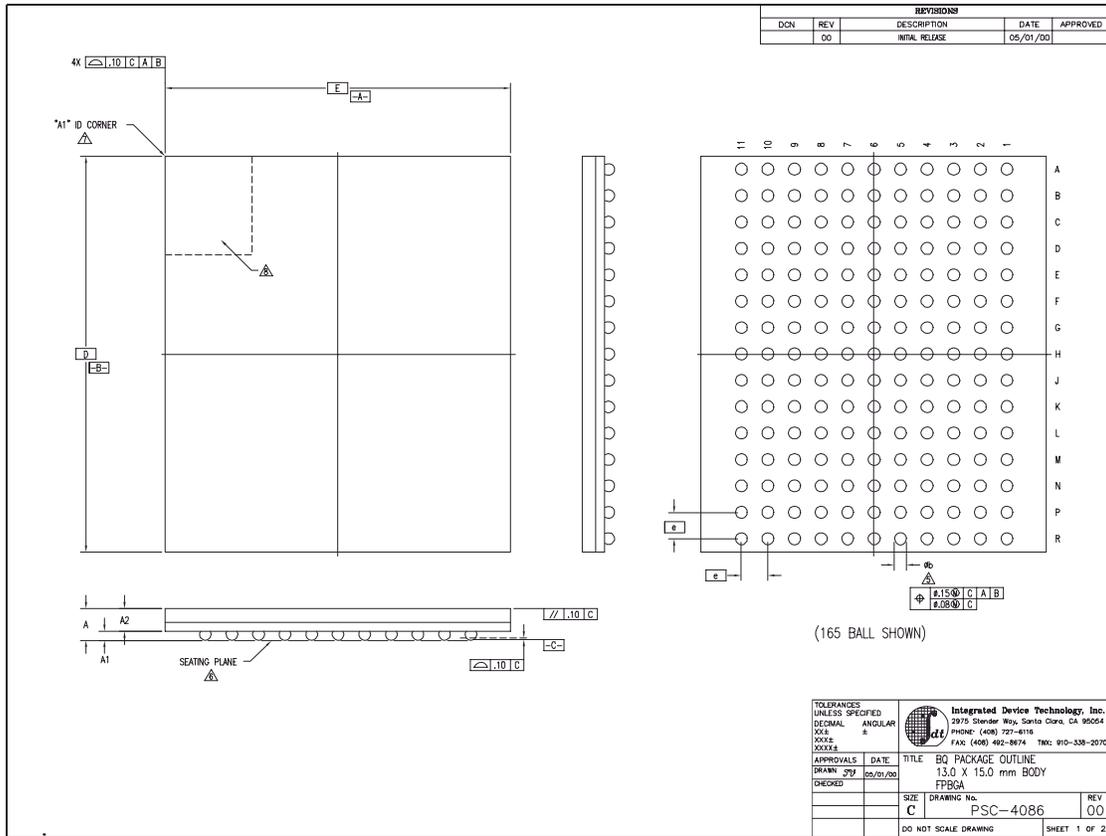
100-Pin Thin Plastic Quad Flatpack (TQFP) Package Diagram Outline



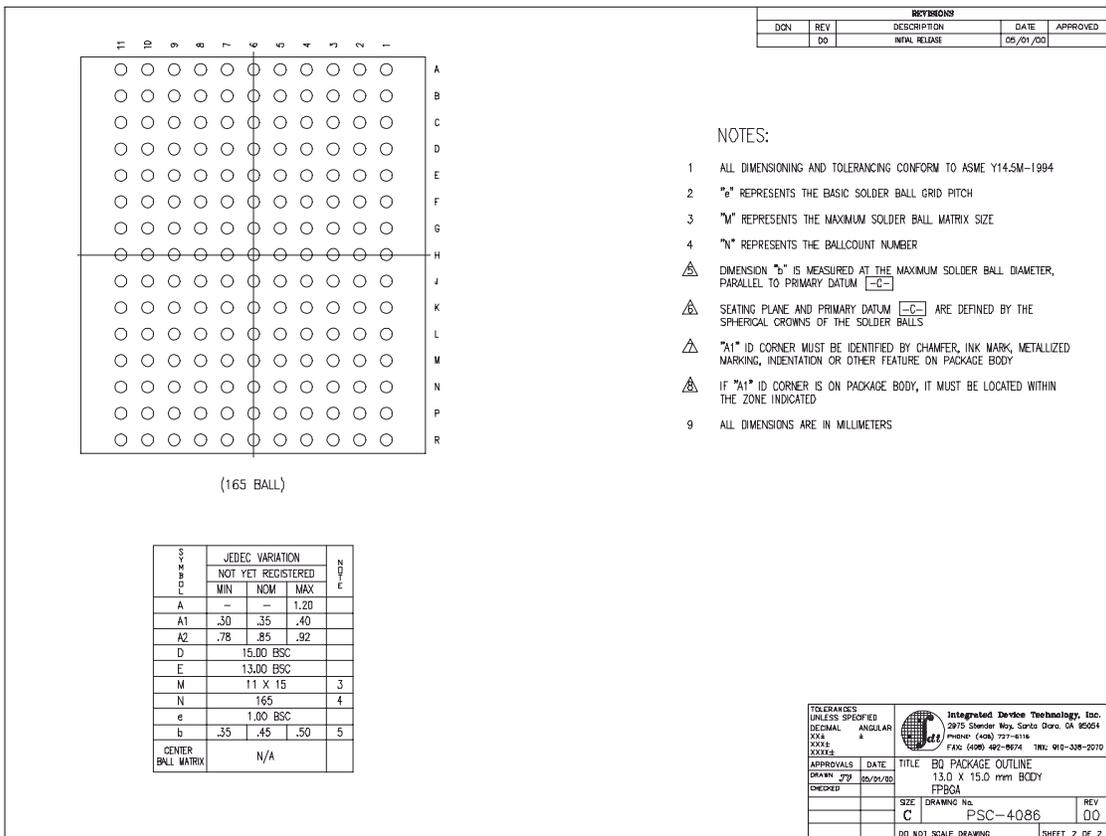
119 Ball Grid Array (BGA) Package Diagram Outline



165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline



| | | | | |
|-----------------------------|----------|--------------------------|---|--------------|
| TOLERANCES UNLESS SPECIFIED | | | Integrated Device Technology, Inc. 2975 Stoner Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TSW: 910-338-2070 | |
| DECIMAL | ANGULAR | | | |
| XXX | ° | | | |
| XXXX | | | | |
| APPROVALS | DATE | TITLE BQ PACKAGE OUTLINE | | |
| DRAWN JYJ | 05/01/00 | 13.0 X 15.0 mm BODY | | |
| CHECKED | | FPBGA | | |
| | | SIZE | DRAWING No. | REV |
| | | C | PSC-4086 | 00 |
| | | DO NOT SCALE DRAWING | | SHEET 1 OF 2 |



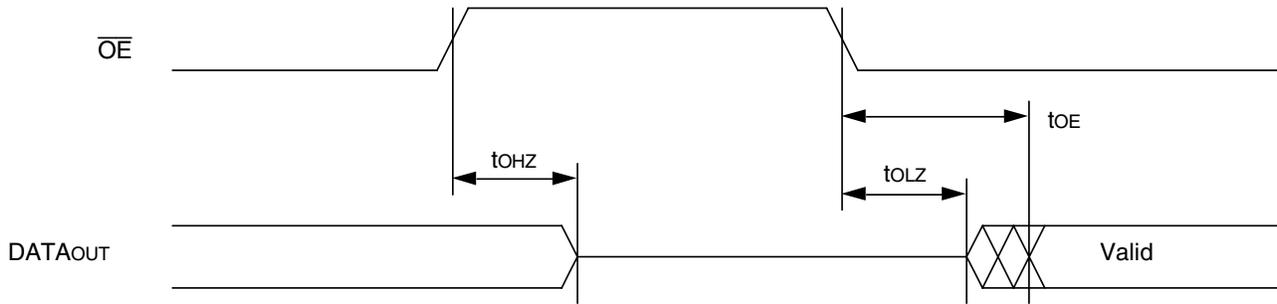
NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2 "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
- 3 "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
- 4 "N" REPRESENTS THE BALLCOUNT NUMBER
- △ DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM [-C-]
- △ SEATING PLANE AND PRIMARY DATUM [-C-] ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
- △ "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
- △ IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED
- 9 ALL DIMENSIONS ARE IN MILLIMETERS

| S M E L | JEDEC VARIATION NOT YET REGISTERED | | | REF N |
|--------------------|---------------------------------------|-----|-----|----------|
| | MIN | NOM | MAX | |
| | A | - | - | |
| A1 | .30 | .35 | .40 | |
| A2 | .78 | .85 | .92 | |
| D | 15.00 BSC | | | |
| E | 13.00 BSC | | | |
| M | 11 X 15 | | | 3 |
| N | 165 | | | 4 |
| e | 1.00 BSC | | | |
| b | .35 | .45 | .50 | 5 |
| CENTER BALL MATRIX | N/A | | | |

| | | | | |
|-----------------------------|----------|--------------------------|---|--------------|
| TOLERANCES UNLESS SPECIFIED | | | Integrated Device Technology, Inc. 2975 Stoner Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TSW: 910-338-2070 | |
| DECIMAL | ANGULAR | | | |
| XXX | ° | | | |
| XXXX | | | | |
| APPROVALS | DATE | TITLE BQ PACKAGE OUTLINE | | |
| DRAWN JYJ | 05/01/00 | 13.0 X 15.0 mm BODY | | |
| CHECKED | | FPBGA | | |
| | | SIZE | DRAWING No. | REV |
| | | C | PSC-4086 | 00 |
| | | DO NOT SCALE DRAWING | | SHEET 2 OF 2 |

Timing Waveform of \overline{OE} Operation⁽¹⁾

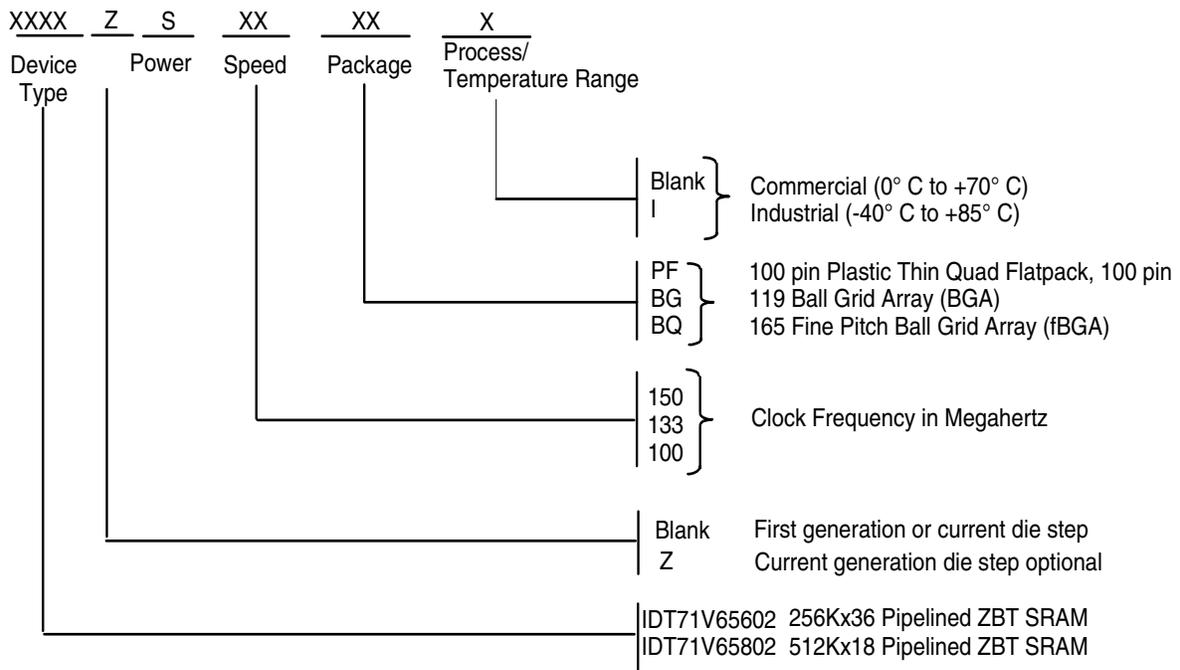


5303 drw 11

NOTE:

1. A read operation is assumed to be in progress.

Ordering Information



5303 drw 12

Datasheet Document History

| | | |
|----------|----------------------|--|
| 12/31/99 | | Created new datasheet from obsolete devices IDT71V656 and IDT71V658 |
| 03/04/00 | Pg. 1, 14, 15 | Removed 166MHz speed grade offering; Added 150MHz speed grade offering |
| 04/20/00 | Pg. 5, 6 | Add JTAG test pins to TQFP pin configuration; removed footnote |
| | | Add clarification note to Recommended Operating Temperature and Absolute Max Ratings tables |
| | Pg. 7 | Add note to BGA Pin configuration; corrected typo in pinout |
| | Pg. 21 | Insert TQFP Package Diagram Outline |
| 05/16/00 | | Add new package offering, 13 x 15mm 165fBGA |
| | Pg. 23 | Correct error in the 119 BGA Package Diagram Outline |
| 07/28/00 | Pg. 5-8 | Remove JTAG pins from TQFP, BG119 and BQ165 pinouts, refer to IDT71V656xx and IDT71V658xx device errata |
| | Pg. 7, 8 | Correct error in pinout, B2 on BG119 and B1 on BQ165 pinout |
| | Pg. 23 | Update BG119 Package Diagram Dimensions |
| 11/04/00 | Pg. 15 | Add I _{ZZ} parameter to DC Electrical Characteristics |
| | Pg. 8 | Add note to pin N5 on the BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$ |
| 12/04/02 | Pg. 1-26 | Changed datasheet from Preliminary to Final Release. |
| | Pg. 5, 6, 15, 16, 25 | Added I temp to datasheet. |
| 12/19/02 | Pg. 1, 2, 5, 6, 7, 8 | Removed JTAG functionality for current die revision. |
| | Pg. 7 | Corrected x36, 119BGA pin configuration. Switched pins I/O0 and I/OP1. |
| 10/15/04 | Pg. 5, 6 | Updated temperature Ta note. |
| | Pg. 7 | Updated pin configuration 512K x 18 for the 119 BGA - reordered I/O signals on P7, N6, L6, K7, H6, G7, F6, E7, D6. |
| 02/21/07 | Pg. 25 | Added Z generation die step to data sheet ordering information. |
| 02/20/09 | Pg. 25 | Removed "IDT" from orderable parts number. |



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