

PM50RL1B120

FLAT-BASE TYPE
INSULATED PACKAGE

PM50RL1B120



FEATURE

Inverter + Brake + Drive & Protection IC

- a) Adopting new 5th generation Full-Gate CSTBT™ chip
- b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.
- c) Error output signal is possible from all each protection upper and lower arm of IPM.
- d) Compatible L-series package.

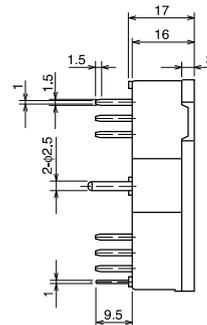
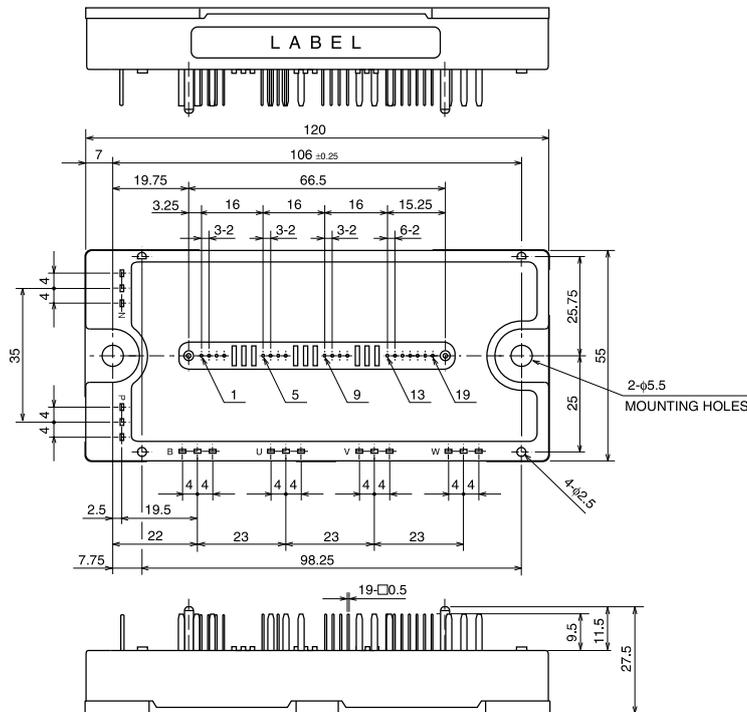
- 3φ 50A, 1200V Current-sense and temperature sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
- UL Recognized

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES

Dimensions in mm



Terminal code

- | | |
|---------|----------|
| 1. VUPC | 11. WP |
| 2. UFO | 12. VWP1 |
| 3. UP | 13. VNC |
| 4. VUP1 | 14. VN1 |
| 5. VVPC | 15. Br |
| 6. VFO | 16. UN |
| 7. VP | 17. VN |
| 8. VVP1 | 18. WN |
| 9. VWPC | 19. Fo |
| 10. WFO | |

PM50RL1B120

FLAT-BASE TYPE
INSULATED PACKAGE

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V Inverter Part, T _j = +125°C Start	800	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value	1000	V
Tstg	Storage Temperature		-40 ~ +125	°C
Viso	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

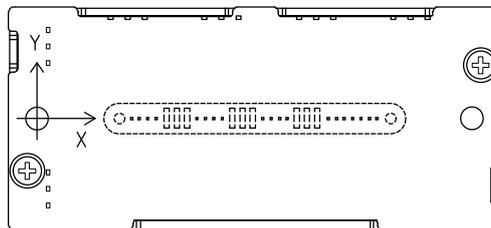
THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element) (Note-1)	—	—	0.27	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1 element) (Note-1)	—	—	0.47	
R _{th(j-c)Q}		Brake IGBT part (Note-1)	—	—	0.39	
R _{th(j-c)F}		Brake FWDi upper part (Note-1)	—	—	0.67	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.038	

* If you use this value, R_{th(f-a)} should be measured just under the chips.

(Note-1) T_c (under the chip) measurement point is below. (unit : mm)

axis \ arm	UP		VP		WP		UN		VN		WN		BR	
	IGBT	FWDi	IGBT	Di										
X	28.6	28.6	65.4	65.4	87.4	87.4	38.6	38.6	54.6	54.6	76.6	76.6	18.0	19.3
Y	-8.4	0.2	-8.4	0.2	-8.4	0.2	6.8	-1.8	6.8	-1.8	6.8	-1.8	-8.9	5.0



Bottom view

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CIN} = 0V, Pulsed (Fig. 1)	—	1.65	2.15	V
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _D = 15V, V _{CIN} = 15V (Fig. 2)	—	2.3	3.3	
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 600V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4)	0.3	0.8	2.0	μs
t _{rr}			—	0.3	0.8	
t _{c(on)}			—	0.4	1.0	
t _{off}			—	1.2	2.8	
t _{c(off)}			—	0.4	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 5)	—	—	1	mA
			—	—	10	

PM50RL1B120

FLAT-BASE TYPE
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BRAKE PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 25A V _{CIN} = 0V, Pulsed (Fig. 1)	T _J = 25°C	—	1.65	2.15	V
			T _J = 125°C	—	1.85	2.35	
V _{EC}	FWDi Forward Voltage	-I _C = 25A, V _{CIN} = 15V, V _D = 15V (Fig. 2)	—	2.3	3.3	V	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 5)	T _J = 25°C	—	—	1	mA
			T _J = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit Current	V _D = 15V, V _{CIN} = 15V	V _{N1} -V _N C	—	8	16	mA
			V*P1-V*PC	—	2	4	
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN • Br-V _N C	1.2	1.5	1.8	V	
V _{th(OFF)}	Input OFF Threshold Voltage		1.7	2.0	2.3		
SC	Short Circuit Trip Level	-20 ≤ T _J ≤ 125°C, V _D = 15V (Fig. 3,6)	Inverter part	100	—	—	A
			Brake part	50	—	—	
t _{off(SC)}	Short Circuit Current Delay Time	V _D = 15V (Fig. 3,6)	—	0.2	—	μs	
OT	Over Temperature Protection	Detect Temperature of IGBT chip	Trip level	135	—	—	°C
			Hysteresis	—	20	—	
UV	Supply Circuit Under-Voltage Protection	-20 ≤ T _J ≤ 125°C	Trip level	11.5	12.0	12.5	V
			Reset level	—	12.5	—	
I _{FO(H)}	Fault Output Current	V _D = 15V, V _{CIN} = 15V (Note-2)	—	—	0.01	mA	
I _{FO(L)}			—	10	15		
t _{FO}	Minimum Fault Output Pulse Width	V _D = 15V (Note-2)	1.0	1.8	—	ms	

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

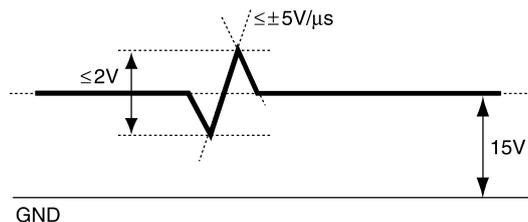
MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	340	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V _D	Control Supply Voltage	Applied between : VUP1-VU _{PC} , VVP1-VV _{PC} VWP1-VW _{PC} , VN1-V _N C (Note-3)	15.0 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN • Br-V _N C	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 9.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-3) With ripple satisfying the following conditions: dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

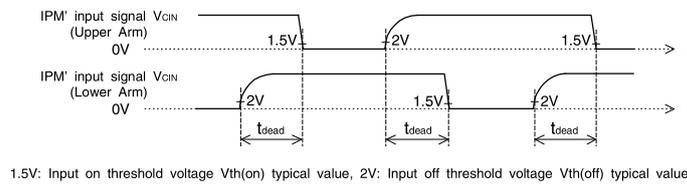
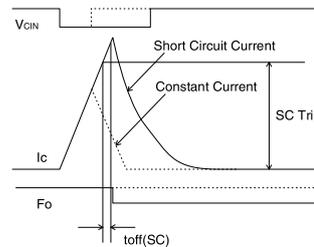
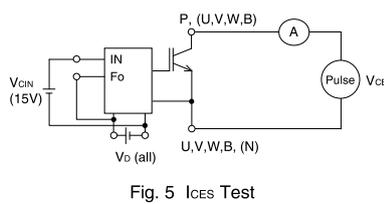
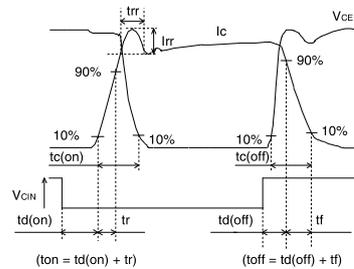
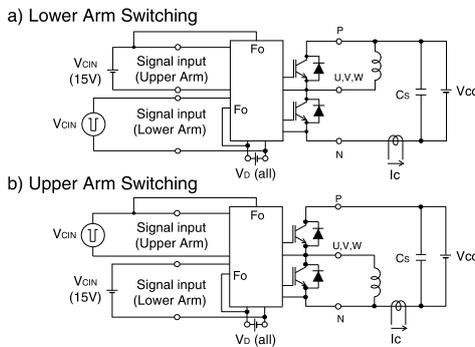
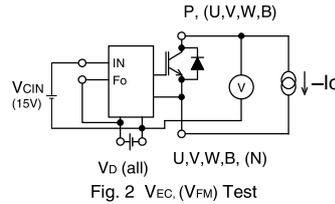
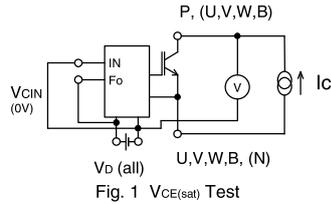


PM50RL1B120

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PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)



PM50RL1B120

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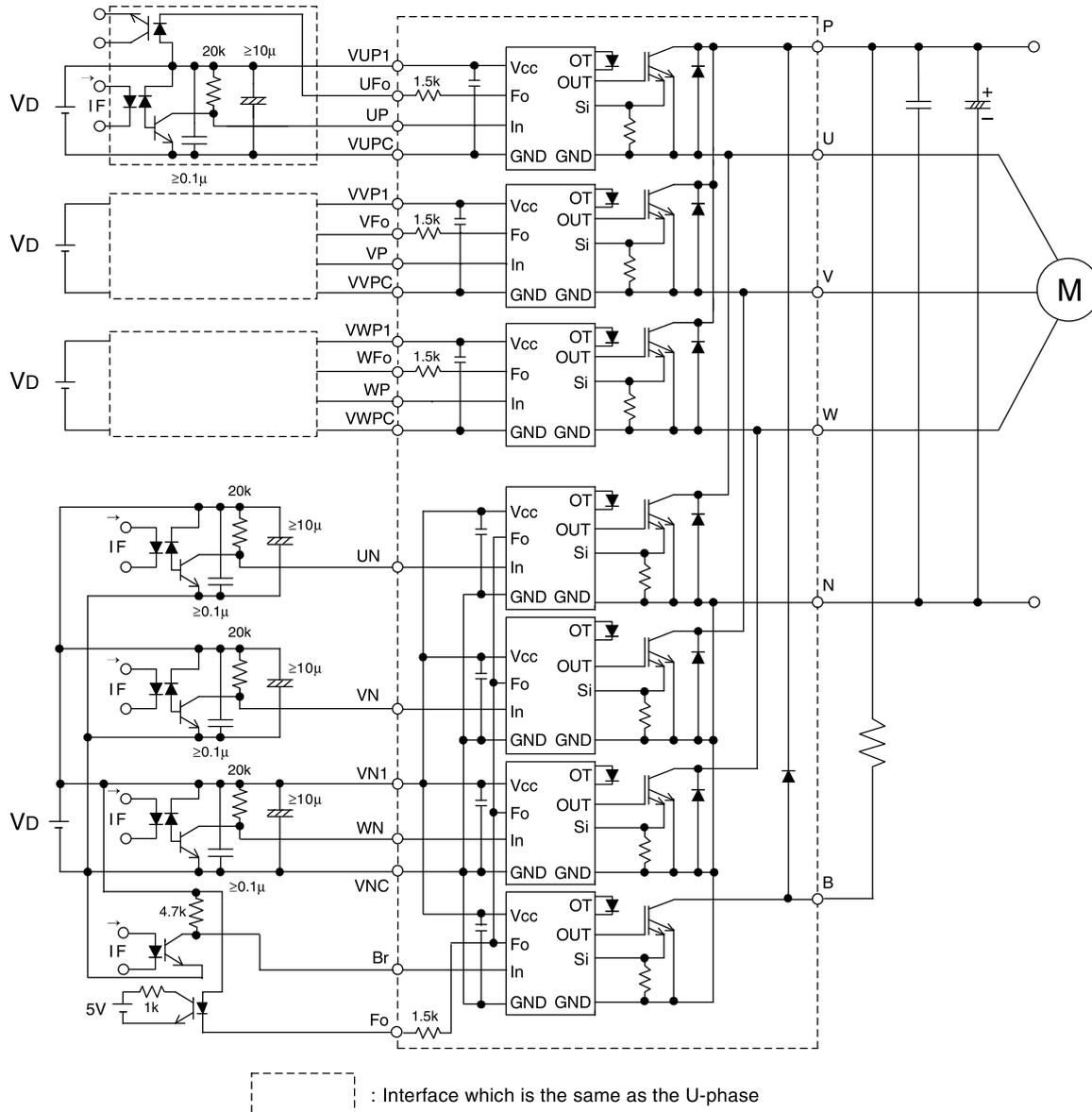


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

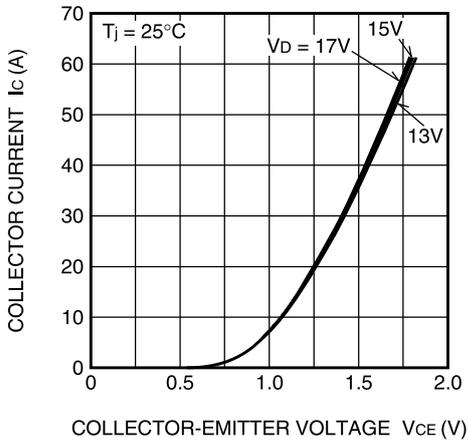
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

PM50RL1B120

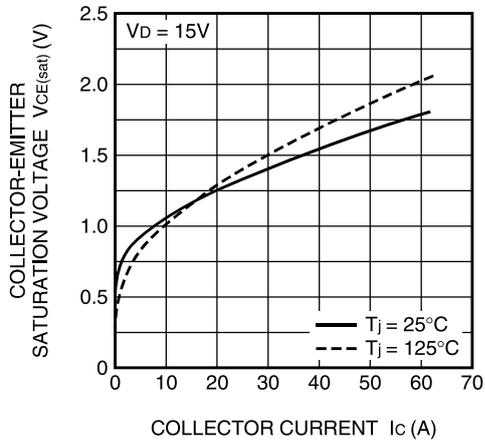
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PERFORMANCE CURVES
(Inverter Part)

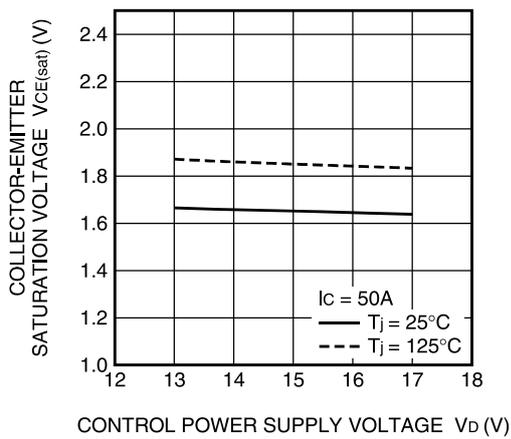
OUTPUT CHARACTERISTICS (TYPICAL)



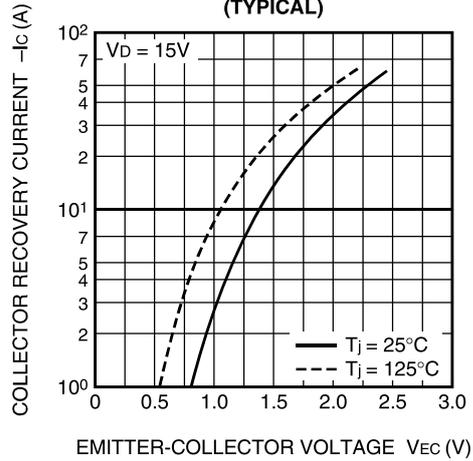
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. I_c) CHARACTERISTICS (TYPICAL)



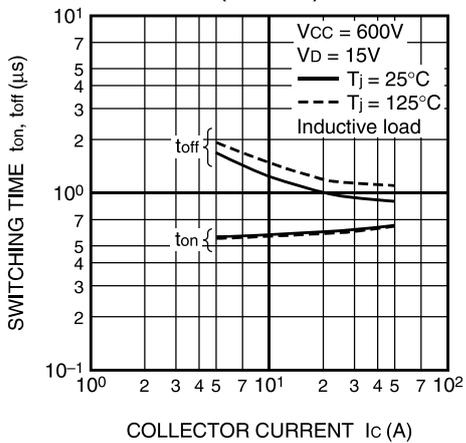
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. V_D) CHARACTERISTICS (TYPICAL)



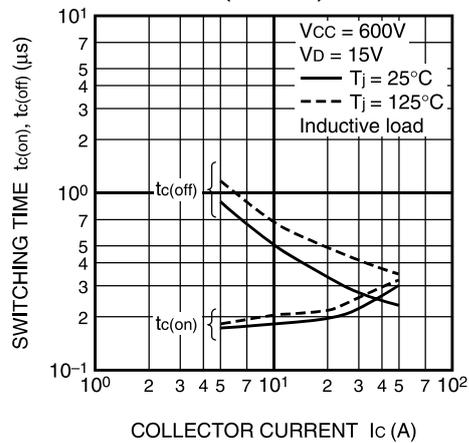
DIODE FORWARD CHARACTERISTICS (TYPICAL)



SWITCHING TIME (t_{on} , t_{off}) CHARACTERISTICS (TYPICAL)



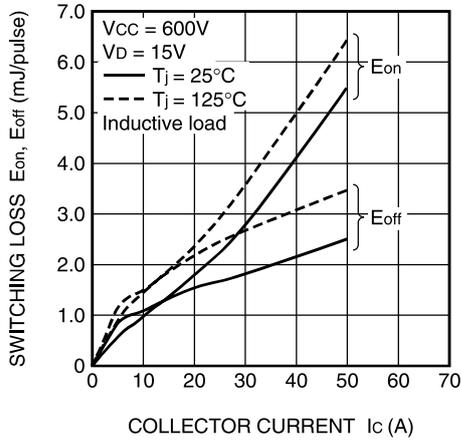
SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



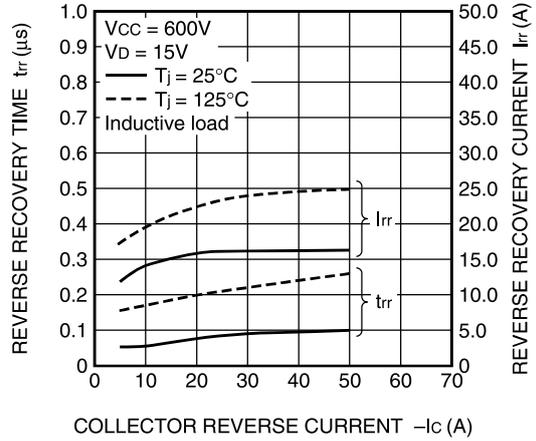
PM50RL1B120

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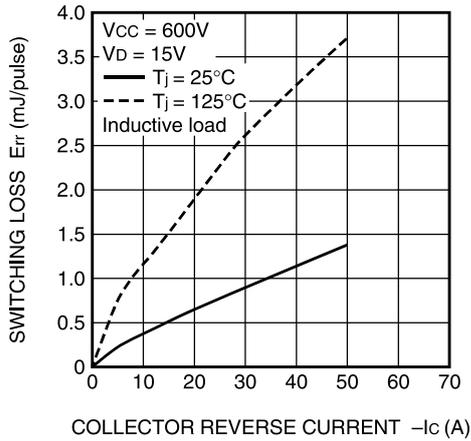
SWITCHING LOSS CHARACTERISTICS (TYPICAL)



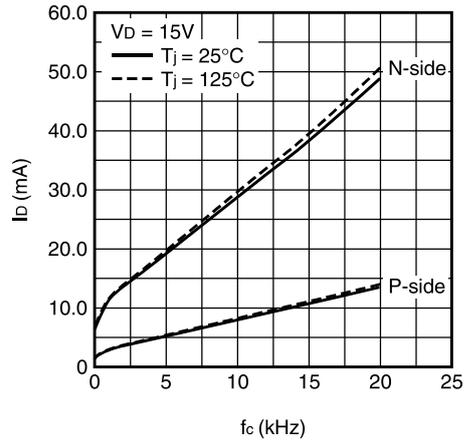
DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



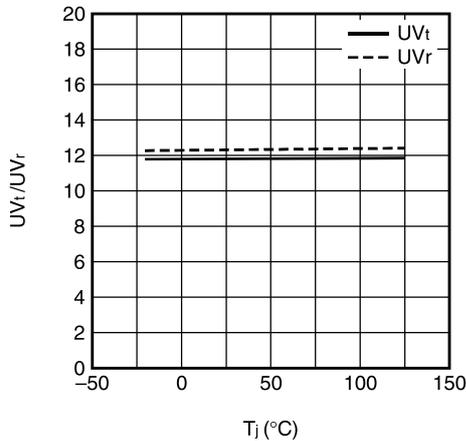
SWITCHING RECOVERY LOSS CHARACTERISTICS (TYPICAL)



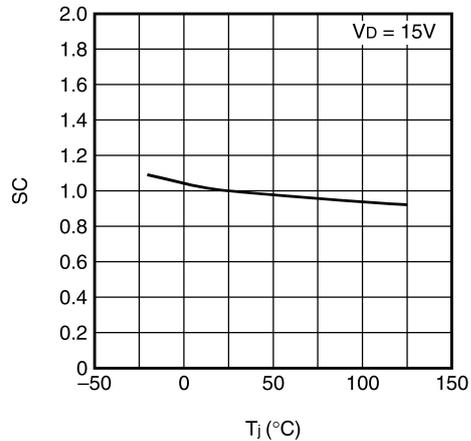
I_D VS. f_c CHARACTERISTICS (TYPICAL)



UV TRIP LEVEL VS. T_j CHARACTERISTICS (TYPICAL)



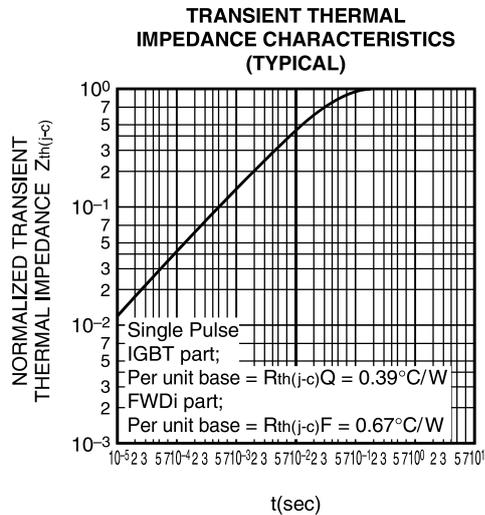
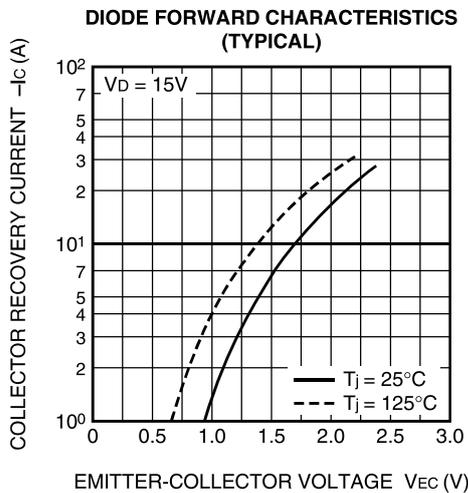
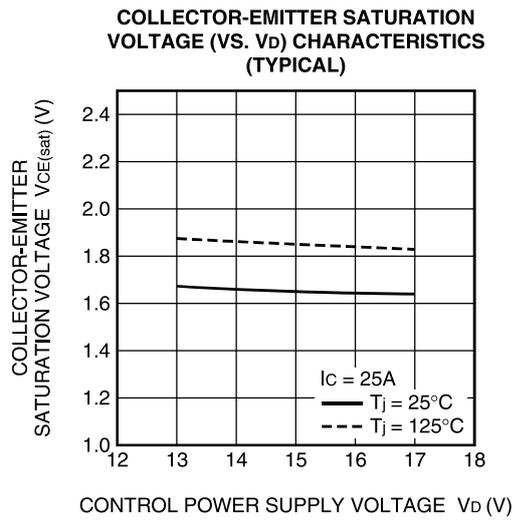
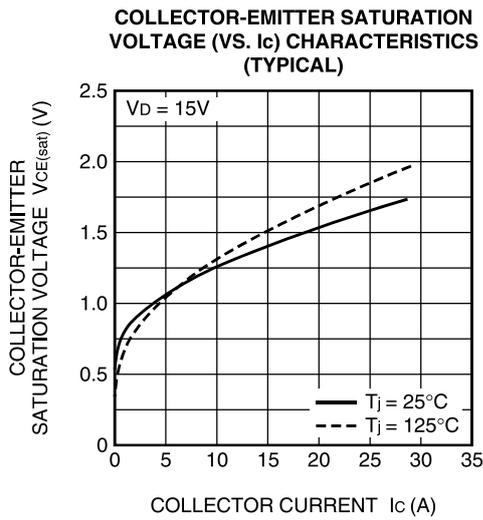
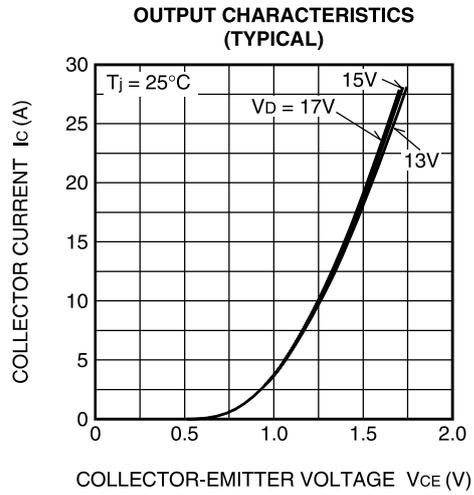
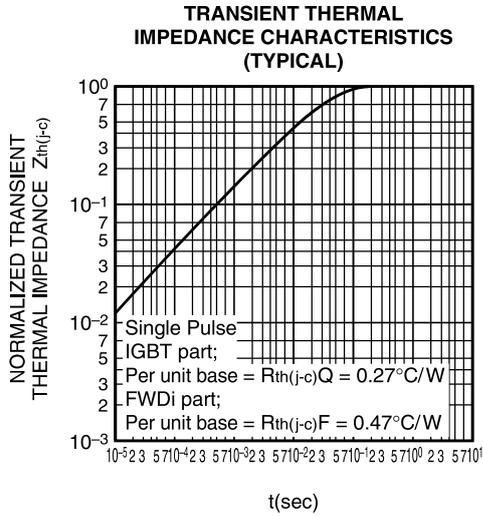
SC TRIP LEVEL VS. T_j CHARACTERISTICS (TYPICAL)



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(Brake Part)



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