

Notification Number:	20230320002.0	Notification Date:	March 21, 2023
Title:	Datasheet for DS90UB953-Q1, DS90UB935-Q1, DS90UB953A-Q1, and TSER953		
Customer Contact:	Notification Manager	Dept:	Quality Services

Change Type: Electrical Specification

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



DS90UB953-Q1

SNLS552D – SEPTEMBER 2017 – REVISED MARCH 2023

Changes from Revision C (October 2020) to Revision D (March 2023) Page

- Typical power consumption bullet on front page updated to match electrical characteristics table..... 1
- IDD_TOTAL typical value changed to 160 mA..... 9
- Changed I2C terminology to "Controller" and "Target"..... 15
- Removed extra arrow from DPHY Receiver to Clock Gen blocks in Functional Block Diagram..... 15
- Added description for non-continuous clock lane mode..... 16
- Added description for deserializer SENSOR_STS registers..... 18
- Updated script example for voltage monitoring..... 20
- Updated description for reading GPIO status when set as output and added GPIO Configuration table.....21
- Added information for enabling Forward Channel GPIO using FC_GPIO_EN.....21
- Updated GPIO Output Control section description for enabling register 0x0E..... 21
- Added typical latency to Forward Channel GPIO table..... 22
- Updated Clocking Mode table with additional modes, frequency clarifications, and CSI-2 bandwidth clarifications..... 22
- Corrected effect of setting M value in register 0x06 35
- Updated description to refer to "DVP_DT_MATCH_EN" in register 0x11. 38
- Changed 0x17[7:4] default value from 0x0 to 0x3..... 39
- Added max and min readings to Voltage Sensor Thresholds description in Register 0x19 39
- Updated SENSOR_V1_THRESH description to match SENSOR_V0_THRESH in register 0x1A..... 40
- Changed "GPIO0 Sensor" to "Internal Temperature Sensor" in register 0x57..... 49
- Changed "FPD3_RX_ID" to "FPD3_TX_ID" in registers 0xF0-0xF5..... 53
- Changed PoC network impedance recommendation from 2 kΩ to 1 kΩ..... 61
- Updated PoC description..... 61
- Removed IL and RL values from Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks Table..... 61
- Changed FB1-FB3 requirement to DCR < 500 mΩ..... 64
- Added note for setting watchdog timer for system initialization..... 68
- Corrected PDB capacitor from 1-μF to 10-μF..... 69

Changes from Revision A (October 2020) to Revision B (March 2023) Page

• Typical power consumption bullet on front page updated to match electrical characteristics table.....	1
• Fixed typo - missing max ambient temp on front page.....	1
• Added note for supply noise frequency range.....	6
• Changed I2C terminology to "Controller" and "Target".....	14
• Removed extra arrow from DPHY Receiver to Clock Gen blocks in Functional Block Diagram.....	14
• Added description for non-continuous clock lane mode.....	15
• Added description for deserializer SENSOR_STS registers.....	17
• Updated script example for voltage monitoring.....	19
• Updated description for reading GPIO status when set as output and added GPIO Configuration table.....	20
• Added information for enabling Forward Channel GPIO using FC_GPIO_EN.....	20
• Updated GPIO Output Control section description for enabling register 0x0E.....	20
• Added typical latency to Forward Channel GPIO table.....	21
• Updated Clocking Mode table with additional modes, frequency clarifications, and CSI-2 bandwidth clarifications.....	21
• Added "set for 4 Gbps line rate" in register 0x05.....	34
• Corrected effect of setting M value in register 0x06	34
• Updated description to refer to "DVP_DT_MATCH_EN" in register 0x11.	37
• Changed 0x17[7:4] default value from 0x0 to 0x3.....	38
• Added max and min readings to Voltage Sensor Thresholds description in Register 0x19	38
• Updated SENSOR_V1_THRESH description to match SENSOR_V0_THRESH in register 0x1A.....	39
• Changed "GPIO0 Sensor" to "Internal Temperature Sensor" in register 0x57.....	48
• Changed "FPD3_RX_ID" to "FPD3_TX_ID" in registers 0xF0-0xF5.....	52
• Changed PoC network impedance recommendation from 2 kΩ to 1 kΩ.....	60
• Updated PoC description.....	60
• Removed IL and RL values from Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks Table.....	60
• Changed FB1-FB3 requirement to DCR < 500 mΩ.....	63
• Added note for setting watchdog timer for system initialization.....	67
• Corrected PDB capacitor from 1-μF to 10-μF.....	68

Changes from Revision A (September 2020) to Revision B (March 2023)**Page**

• Typical power consumption bullet on front page updated to match electrical characteristics table.....	1
• Changed I2C terminology to "Controller" and "Target".....	13
• Removed extra arrow from DPHY Receiver to Clock Gen blocks in Functional Block Diagram.....	13
• Added description for non-continuous clock lane mode.....	14
• Added description for deserializer SENSOR_STS registers.....	16
• Updated script example for voltage monitoring.....	18
• Updated description for reading GPIO status when set as output and added GPIO Configuration table.....	19
• Added information for enabling Forward Channel GPIO using FC_GPIO_EN.....	19
• Updated GPIO Output Control section description for enabling register 0x0E.....	19
• Added typical latency to Forward Channel GPIO table.....	20
• Updated Clocking Mode table with additional modes, frequency clarifications, and CSI-2 bandwidth clarifications.....	20
• Corrected effect of setting M value in register 0x06.....	33
• Updated description to refer to "DVP_DT_MATCH_EN" in register 0x11.....	36
• Changed 0x17[7:4] default value from 0x0 to 0x3.....	37
• Added max and min readings to Voltage Sensor Thresholds description in Register 0x19.....	38
• Updated SENSOR_V1_THRESH description to match SENSOR_V0_THRESH in register 0x1A.....	38
• Changed "GPIO0 Sensor" to "Internal Temperature Sensor" in register 0x57.....	50
• Changed "FPD3_RX_ID" to "FPD3_TX_ID" in registers 0xF0-0xF5.....	58
• Changed PoC network impedance recommendation from 2 kΩ to 1 kΩ.....	65
• Updated PoC description.....	65
• Removed IL and RL values from Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks Table.....	65
• Changed FB1-FB3 requirement to DCR < 500 mΩ.....	68
• Added note for setting watchdog timer for system initialization.....	72
• Corrected PDB capacitor from 1-μF to 10-μF.....	73

**TSER953**

SNLS696B – APRIL 2021 – REVISED MARCH 2023

Changes from Revision A (May 2021) to Revision B (March 2023)**Page**

• Typical power consumption bullet on front page updated to match electrical characteristics table.....	1
• Added note for supply noise frequency range.....	7
• IDD_TOTAL typical value changed to 160 mA.....	8
• Changed I2C terminology to "Controller" and "Target".....	13
• Removed extra arrow from DPHY Receiver to Clock Gen blocks in Functional Block Diagram.....	13
• Added description for non-continuous clock lane mode.....	14
• Added description for deserializer SENSOR_STS registers.....	16
• Updated script example for voltage monitoring.....	18
• Updated description for reading GPIO status when set as output and added GPIO Configuration table.....	19
• Added information for enabling Forward Channel GPIO using FC_GPIO_EN.....	19
• Updated GPIO Output Control section description for enabling register 0x0E.....	20
• Added typical latency to Forward Channel GPIO Typical Timing table.....	21
• Updated Clocking Mode table with additional modes, frequency clarifications, and CSI-2 bandwidth clarifications.....	21
• Corrected effect of setting M value in register 0x06.....	33
• Added max and min readings to Voltage Sensor Thresholds description in Register 0x19.....	38
• Updated SENSOR_V1_THRESH description to match SENSOR_V0_THRESH in register 0x1A.....	38
• Changed "GPIO0 Sensor" to "Internal Temperature Sensor" in register 0x57.....	49
• V3LINK_RX_ID changed to V3LINK_TX_ID in register 0xF0-0xF5.....	57
• Removed IL and RL values from Suggested Components for a "4G" V ³ Link PoC Network Table.....	65
• Changed PoC network impedance recommendation from 2 kΩ to 1 kΩ.....	65
• Updated PoC description.....	65
• Changed PDB capacitor value to "> 10 μF".....	68
• Changed PDB capacitor value from 1-μF to 10-μF.....	73

The datasheet number will be changing.

Device Family	Change From:	Change To:
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DS90UB953-Q1	SNLS552C	SNLS552D
DS90UB935-Q1	SNLS605A	SNLS605B
DS90UB953A-Q1	SNLS643A	SNLS643B
TSER953	SNLS696A	SNLS696B

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/DS90UB953-Q1>

<http://www.ti.com/product/DS90UB935-Q1>

<http://www.ti.com/product/DS90UB953A-Q1>

<http://www.ti.com/product/TSER953>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:

DS90UB953TRHBRQ1	DS90UB953TRHBTQ1	DS90UB935TRHBRQ1	DS90UB935TRHBTQ1
DS90UB953ATRHBRQ1	DS90UB953ATRHBTQ1	TSER953RHBR	TSER953RHBT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
WW Change Management Team	PCN_ww_admin_team@list.ti.com

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