

CMOS Digital Integrated Circuits Silicon Monolithic

74VHC9151FT,74VHC9152FT

1. Functional Description

74VHC9151FT: 9-BIT SCHMITT BUFFER

74VHC9152FT: 9-BIT SCHMITT INVERTER

2. General

The 74VHC9151FT/74VHC9152FT are an ultra-high-speed 9-bit Schmitt Buffer / Inverter fabricated using silicon-gate CMOS technology. The 74VHC9151FT/74VHC9152FT combines low power consumption of CMOS with Schottky TTL speeds.

74VHC9151FT output is a non-inverting type and the 74VHC9152FT output is an inverting type.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHC9151FT/74VHC9152FT are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Additionally, all the inputs have a newly developed protection circuit without a diode returned to V_{CC} . This enables the inputs to be tolerant of up to 5 volts even when power supply is down.

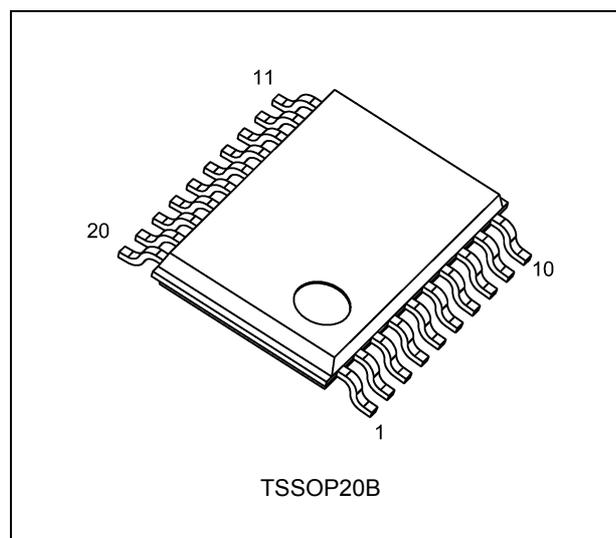
The input power-down protection capability makes the 74VHC9151FT/74VHC9152FT ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125 °C
- (3) High speed: $t_{pd} = 3.6$ ns (typ.) at $V_{CC} = 5.0$ V
- (4) Low power dissipation: $I_{CC} = 4.0$ μ A (max) at $T_a = 25$ °C
- (5) Power down protection is provided on all inputs.
- (6) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (7) Wide operating voltage range: $V_{CC(opr)} = 2.0$ V to 5.5 V

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

4. Packaging

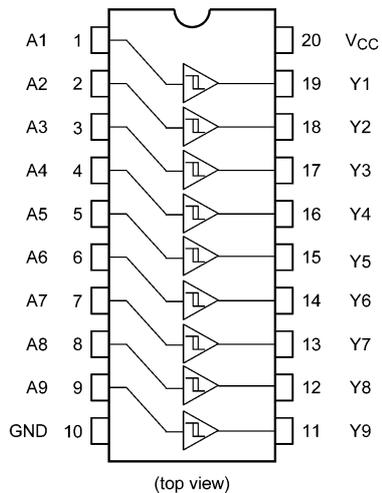


Start of commercial production

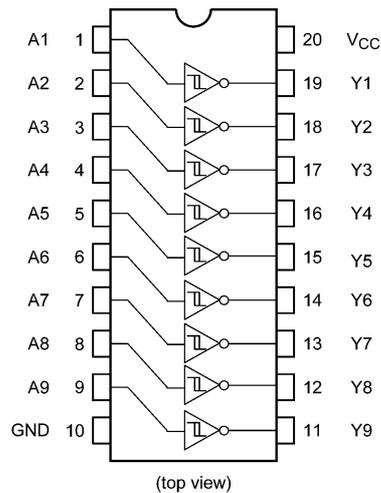
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5. Pin Assignment

74VHC9151FT

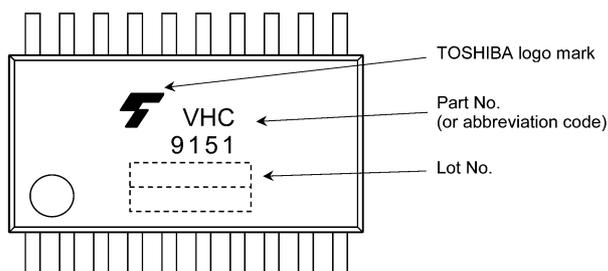


74VHC9152FT

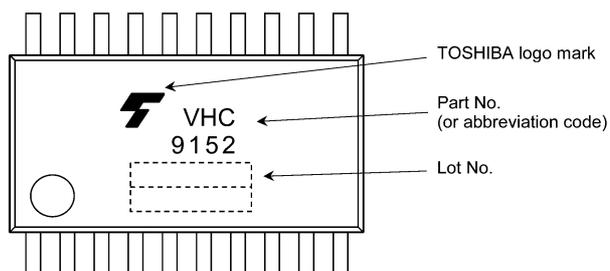


6. Marking

74VHC9151FT



74VHC9152FT



7. Truth Table

A	Y 74VHC9151FT	Y 74VHC9152FT
L	L	H
H	H	L

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}		-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}		± 20	mA
Output current	I_{OUT}		± 25	mA
V_{CC} /ground current	I_{CC}		± 75	mA
Power dissipation	P_D	(Note 1)	180	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of $T_a = -40$ to 85 °C. From $T_a = 85$ to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

9. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 125	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit	
Positive threshold voltage	V_P	—	3.0	—	—	2.20	V	
			4.5	—	—	3.15		
			5.5	—	—	3.85		
Negative threshold voltage	V_N	—	3.0	0.90	—	—	V	
			4.5	1.35	—	—		
			5.5	1.65	—	—		
Hysteresis voltage	V_H	—	3.0	0.30	—	1.20	V	
			4.5	0.40	—	1.40		
			5.5	0.50	—	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
				4.5	3.94	—	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
				4.5	—	—	0.36	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	± 0.1	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	μA	

10.2. DC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
Positive threshold voltage	V_P	—	3.0	—	2.20	V	
			4.5	—	3.15		
			5.5	—	3.85		
Negative threshold voltage	V_N	—	3.0	0.90	—	V	
			4.5	1.35	—		
			5.5	1.65	—		
Hysteresis voltage	V_H	—	3.0	0.30	1.20	V	
			4.5	0.40	1.40		
			5.5	0.50	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
				4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
				4.5	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	μA	

10.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit	
Positive threshold voltage	V_P	—		3.0	—	2.20	V	
				4.5	—	3.15		
				5.5	—	3.85		
Negative threshold voltage	V_N	—		3.0	0.90	—	V	
				4.5	1.35	—		
				5.5	1.65	—		
Hysteresis voltage	V_H	—		3.0	0.30	1.20	V	
				4.5	0.40	1.40		
				5.5	0.50	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μ A	2.0	1.9	—	V	
				3.0	2.9	—		
				4.5	4.4	—		
				$I_{OH} = -4$ mA	3.0	2.40		—
				$I_{OH} = -8$ mA	4.5	3.70		—
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μ A	2.0	—	0.1	V	
				3.0	—	0.1		
				4.5	—	0.1		
				$I_{OL} = 4$ mA	3.0	—		0.55
				$I_{OL} = 8$ mA	4.5	—		0.55
Input leakage current	I_{IN}	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	± 2.0	μ A	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	80.0	μ A	

10.4. AC Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	74VHC9151FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	4.8	9.4	ns
						50	—	8.1	16.1	
					5.0 ± 0.5	15	—	3.3	6.0	
						50	—	5.7	10.5	
Propagation delay time	74VHC9152FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	4.8	9.3	ns
						50	—	7.8	15.4	
					5.0 ± 0.5	15	—	3.6	6.3	
						50	—	5.7	10.2	
Output skew		t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	ns
					5.0 ± 0.5	50	—	—	1.0	
Input capacitance		C_{IN}		—			—	4	10	pF
Power dissipation capacitance	74VHC9151FT	C_{PD}	(Note 2)	$f_{IN} = 1$ MHz			—	11	—	pF
	74VHC9152FT						—	10	—	

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHM} - t_{PLHN}|$, $t_{osHL} = |t_{PHLM} - t_{PHLN}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/9 \text{ (per bit)}$$

10.5. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC9151FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	10.7	ns
						50	1.0	18.4	
					5.0 ± 0.5	15	1.0	6.8	
						50	1.0	11.9	
Propagation delay time	74VHC9152FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	10.6	ns
						50	1.0	17.6	
					5.0 ± 0.5	15	1.0	7.1	
						50	1.0	11.6	
Output skew		t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHM} - t_{PLHN}|$, $t_{osHL} = |t_{PHLM} - t_{PHLN}|$)

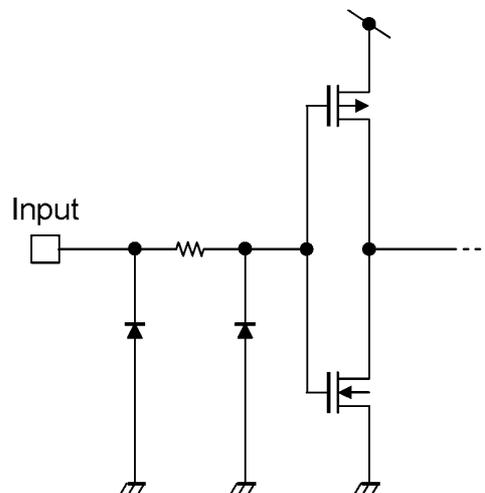
10.6. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC9151FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	12.0	ns
						50	1.0	20.0	
					5.0 ± 0.5	15	1.0	7.5	
						50	1.0	13.0	
Propagation delay time	74VHC9152FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	11.5	ns
						50	1.0	19.5	
					5.0 ± 0.5	15	1.0	8.0	
						50	1.0	13.0	
Output skew		t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHM} - t_{PLHN}|$, $t_{osHL} = |t_{PHLM} - t_{PHLN}|$)

11. Internal Equivalent Circuit



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