Differences between Cinterion® PLS8, PDS5/6/8 and PLS62-W

Migration Guide

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0 Document History

Preceding Document:
"Differences between Cinterion® PLS8, PDS5/6/8 and PLS62-W", Version 01
New document:
"Differences between Cinterion® PLS8, PDS5/6/8 and PLS62-W", Version 02

Chapter	What is new
3.2.14	Revised Table 16 and Table 17

New document:
"Differences between Cinterion® PLS8, PDS5/6/8 and PLS62-W", Version 01

Chapter	What is new
---	Initial document setup.

1 Introduction

This document[1] compares the Gemalto M2M modules PLS8 Rel. 3 with PDS5, PDS6 and PDS8 and PLS62-W. It lists hardware related differences between these modules.

The aim of the document is to provide guidance on how to migrate from PLS8, PDS5/6/8 to PLS62-W. Chapter 4 gives advice on designing one common hardware platform for smooth transition between all described products.

PLS8 in this document refers to the product variants PLS8-E, PLS8-US, PLS8-V and PLS8-X. Where necessary a note is made to differentiate between these product variants.

PDS5 in this document refers to the product variants PDS5-E and PDS5-US. Where necessary a note is made to differentiate between these two product variants.

1.1 Related Documents

[1] PLS8 Hardware Interface Description
[2] PDS5 Hardware Interface Description
[3] PDS6 Hardware Interface Description
[4] PDS8 Hardware Interface Description
[5] PLS62-W Hardware Interface Description
[6] PLS8 AT Command Set
[7] PDS5 AT Command Set
[8] PDS6 AT Command Set
[9] PDS8 AT Command Set
[10] PLS62-W AT Command Set

1.2 Type Approval

PLS8, PDS5, PDS6, PDS8 and PLS62 comply with the same standards and directives – except for

- Standards of North American type approval that are not applicable to PHS8-E and PDS5-E
- Standards of European type approval that are not applicable to PLS8-US, PLS8-V, PLS8-X and PDS5-US

For more regulatory and type approval information see [1], [2], [3], [4] and [5].

[1] The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Gemalto M2M product.

2 Software Related Differences

For a complete overview of all AT command differences between all products please refer to the specific AT Command Specifications. See list in Section 1.1 “Related Documents”.

3 Hardware Related Differences

The focus of this chapter is on hardware differences between PLS8, PDS5, PDS6, PDS8 and PLS62.

3.1 Feature Overview

The following table compares general properties and features of PLS8, PDS5, PDS6, PDS8 and PLS62-W.
It lists differences between the modules. Where appropriate, these differences are described in more detail in the next sections.

Table 1: Feature overview

Feature/Property	PLS8	PDS5	PDS6	PDS8	PLS62-W
General Properties					
Power supply ratings	For details see Section 3.2.7				
Operating temperature (board temperature)	Normal operation: -30°C to +85°C Extended operation: -40°C to +95°C	Normal operation: -30°C to +85°C Extended operation: -40°C to +90°C			
Dimensions	33mm x 29mm x 2.2mm Weight: approx.4.5g	33mm x 29mm x 2.3mm Weight: approx.5g			33mm x 29mm x 3.06mm Weight: approx.5g
Frequency bands GSM [MHz]	PLS8-E, PLS8-US, PLS8-X: Quad band, 850/900/1800/1900 PLS8-V: not supported	PDS5-E: Dual band, 900/1800 PDS5-US: Dual band, 850/1900	Quad band, 850/900/1800/1900		
Frequency Bands UMTS/HSPA+ [MHz]	PLS8-E: Triple band, 900/1800/2100 PLS8-US, PLS8-X: Triple band, 850/ AWS/1900 PLS8-V: not supported	PDS5-E: Dual band, 900/2100 PDS5-US: Dual band, 850/1900	Five band, 800 (BdVI) / 850 (BdV) / 900 (BdVIII) / 1900 (BdII) / 2100 (BdI)		Seven band, 800 (BdXIX) / 850 (BdV) / 900 (BdVIII) / AWS (BdIV) / 1800 (BdIX) / 1900 (BdII) / 2100 (BdI)

Feature/Property	PLS8	PDS5	PDS6	PDS8	PLS62-W
Frequency Bands LTE [MHz]	PLS8-E: Five band, 800 (Bd20) / 900 (Bd8) / 1800 (Bd3) / 2100 (Bd1) / 2600 (Bd7) PLS8-US: Quad band, 700 (Bd17) / 850 (Bd5) / AWS (Bd4) / 1900 (Bd2) PLS8-X: Five band, 700 (Bd13 + Bd17) / 850 (Bd5) / AWS (Bd4) / 1900 (Bd2) PLS8-V: Triple Band, 700 (Bd13) / AWS (Bd4) / 1900 (Bd2)	not supported			Twelve band, 700 (Bd12 <MFBI Bd17>, Bd28) / 800 (Bd18, Bd19,Bd20) / 850 (Bd5) / 900 (Bd8) / AWS (Bd4) / 1800 (Bd3) / 1900 (Bd2) / 2100 (Bd1) / 2600 (Bd7)
Interface Properties					
Number of pads	156 pads. For pad assignment see Chapter 4.				
SIM Interface	1				2
Serial Interfaces					
Serial interface ASC0	Baudrate: 115,200bps Flow control: RTS0/CTS0 Signal level: 1.8V	Baudrate: 1,200 to 921,600bps Autobauding: 1,200bps to 230,400bps Flow control: RTS0/CTS0 Signal level: 1.8V			Baudrate: 1,200 to 921,600bps Autobauding: 1,200bps to 230,400bps Flow control: RTS0/CTS0 Signal level: 1.8V

Feature/Property	PLS8	PDS5	PDS6	PDS8	PLS62-W
ASC1	Not supported	Not supported			Baudrate: 1,200 to 921,600bps Autobauding: 1,200bps to 230,400bps Flow control: RTS1/CTS1 Signal level: 1.8V
USB interface	USB 2.0 High Speed (480Mbit/s) device interface	USB 2.0 High Speed (480Mbit/s) device interface, Full Speed (12Mbit/s) compliant			
Interface configuration	AT^SSRVSET assigns the module's interfaces USB0 – USB4, ASC0 and Multiplex channels 1 – 4 to available services: two AT command instances MDM and APP, NMEA Streaming. Provides a number of predefined and customizable service sets. Multiplexer can be started on MDM instance.	AT^SCFG "Serial/Interface/Allocation" command: Provides 3 fixed interface configurations. Assigns AT command instances and trace instances to the module's devices USB0, USB1, USB2 (only tracing), USB3 and ASC0. No dedicated AT command instances MDM / APP like PLS8. PDS8: NMEA not dedicated, can be assigned to any AT command instance by using AT^SGPSC. One USB composite enumeration: • USB CDC-ACM with several ports • No WWAN adapter supported. Multiplexer can be started on ASC0, USB0, USB3. On USB1 only if "Serial/Interface/Allocation" 2.			AT^SSRVSET assigns the module's interfaces USB5 and USB6 to available services: USB0: Modem USB1/2: ACM, AT channel USB3: ACM, trace channel USB4: reserve USB5: ECM/NCM or MBIM USB6: ECM/NCM
Audio interfaces					
Analogue audio	Not supported	Not supported	One balanced audio interface	Not supported	Not supported
Digital audio	PCM or I^2S	PCM			PCM (prepared)
RTC backup	Yes, 1.5V < VDDLP < 3.25V	Yes, 1.0V < VDDLP < 1.9V			

Feature/Property	PLS8	PDS5	PDS6	PDS8	PLS62-W
GPIO interface	10 GPIO lines. GPIO6 shared with Low Current Indicator LC_IND.	8 GPIO lines. GPIO4 shared with Fast Shutdown and Host wakeup line WAKEUP Additional functions: GPIO6, GPIO7: PWM GPIO8: Counter			24 GPIO lines 14 lines shared with ASC0, ASC1 and SPI lines, with network status indication, PWM functionality, fast shutdown, pulse counter, and SIM switch 10 GPIO lines not shared
SPI interface	Not supported	supported			
I2C interface	Not supported	supported			
Antenna	50 Ohm. Main GSM/UMTS/LTE antenna. UMTS/LTE diversity antenna. GNSS antenna (active/passive)	50 Ohm. GSM/UMTS antenna.		50 Ohm. GSM/UMTS antenna. GNSS antenna (active/passive)	50 Ohm. Main GSM/UMTS/LTE antenna. UMTS/LTE diversity antenna.
Ignition signal	ON: Low impulse >100ms	ON: Low pulse >300ms			ON: falling edge
ADC inputs	3 ADC	1 ADC			
GNSS	Supported (GPS/GLONASS)	Not supported	Not supported	Supported (GPS)	Not supported
Other Properties					
HSPA	UE CAT. 14, 24 DC-HSPA+ – DL 42Mbps HSUPA – UL 5.76Mbps Compressed mode (CM) supported according to 3GPP TS25.212	DL 7.2Mbps, UL 5.7Mbps HSDPA Cat.8 / HSUPA Cat.6 data rates Compressed mode (CM) supported according to 3GPP TS25.212			DL 7.2Mbps, UL 5.7Mbps HSDPA Cat.8 / HSUPA Cat.6 data rates Compressed mode (CM) supported according to 3GPP TS25.212
LTE	UE CAT 3 supported DL 100Mbps, UL 50Mbps 2x2 MIMO in DL direction	Not supported			UE CAT 1 supported DL 10.2Mbps, UL 5.2Mbps
UMTS	PS data rate: 384 kbps DL / 384 kbps UL	PS data rate: 384 kbps DL / 384 kbps UL			

Feature/Property	PLS8	PDS5	PDS6	PDS8	PLS62-W
		CS data rate: 64 kbps DL / 64 kbps UL			
EGPRS	Multislot class 12				
GPRS	Multislot class 12				
For software related differences please refer to [6], [7], [8], [9] and [10].					

3.2 Application Interface

3.2.1 IGT Signal

The IGT signal starts the module. Differences are shown in the following table. It is recommended for all modules to drive this line low by an open drain or open collector driver connected to GND.

Table 2: Electrical characteristics of IGT signal

Signal	PLS8	PDS5	PDS6	PSD8	PLS62-W
R_{PU}	≈ 200kΩ	≈ 100kΩ			
V_{IH}max	2.2V	VDDLPmax			
V_{IH}min	1.17V	1.8V			1.3V
V_{IL}max	0.3V	0.5V			
Input sensitivity	Low pulse (>100ms)	Low pulse (>300ms)			Falling edge Slew rate ≤ 1ms

Reference:
- "Hardware Interface Description": Section "Pad Assignment and Signal Description"

3.2.2 EMERG_OFF

The emergency off signal switches the module immediately off and causes the loss of all information stored in the volatile memory. Therefore the EMERG_OFF line should only be used when, due to serious problems, the software is not responding for more than 5 seconds.

EMERG_OFF should be externally driven by an open collector or open drain driver.

Table 3: EMERG_OFF characteristics

Signal	PLS8	PDS5	PDS6	PSD8	PLS62-W
R_{PU}	≈ 40kΩ	≈ 1kΩ, C_I ≈ 1nF			
V_{IH}max	2.1V	VDDLPmax			
V_{IH}min	1.17V	1.35V			
V_{IL}max	0.3V	0.3V			
Input sensitivity	Low pulse (>40ms)	Low pulse (>20ms)			Low pulse (>20ms)

Reference:
- "Hardware Interface Description": Section "Pad Assignment and Signal Description"

3.2.3 Power Supply BATT+

The module power supply needs an external interference suppression capacitor at all power supply domains. The name and purpose of power supply domain and values of the interference suppression capacitors are shown in Table 4.

Table 4: BATT+ power supply and interference suppression

Pad	PHS8	PDS5	PDS6	PSD8	PLS62-W
N13, P13	BATT+ µC and LDOs > 47µF XR5 MLCC	BATT+ µC and LDOs > 150µF XR5 MLCC			BATT+BB µC and LDOs ≥ 150µF XR5 MLCC
N3, N4	BATT+_RF For all PAs > 4x47µF XR5 MLCC	BATT+_RF For all PAs > 150µF XR5 MLCC			BATT+RF For all Pas ≥ 150µF XR5 MLCC
A4, B3	Not connected				Not connected

The following figures show a possible external interference suppression circuits.

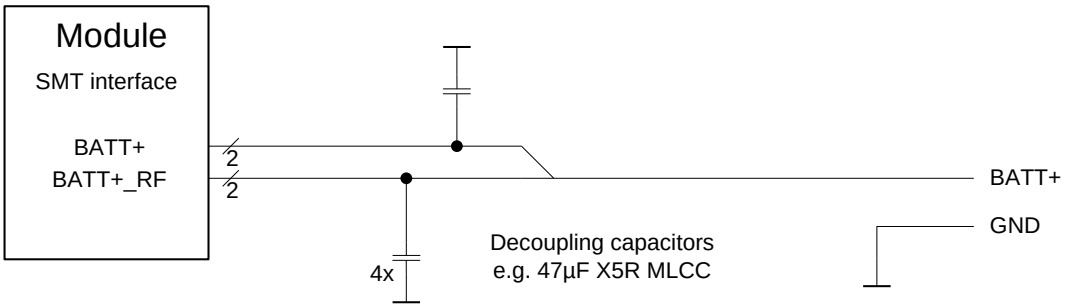


Figure 1: Decoupling capacitors for BATT+ for PLS8

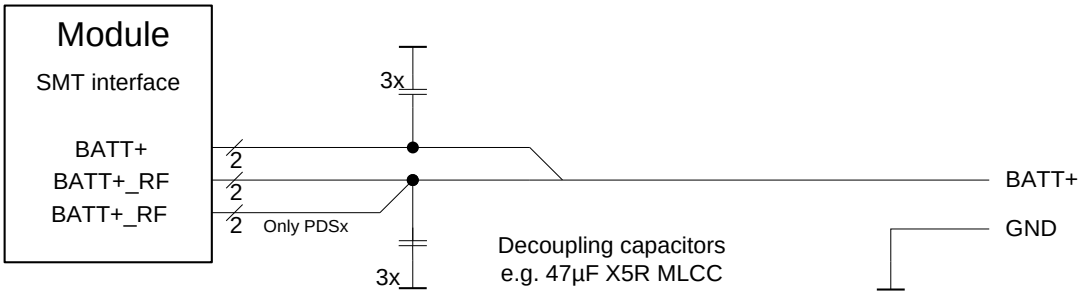


Figure 2: Decoupling capacitors for BATT+ for PDS5, PDS6 PDS8 and PLS62

3.2.4 Voltage Domain VEXT/V180

All modules support VEXT to supply external HW connected to the module.
PHS8 supports a power save mode, which can be controlled by AT^SCFG="MEopMode/PowerMgmt/VExt" (see [6]).

Table 5: BATT+ power supply and interference suppression

VEXT/V180	PLS8	PDS5	PDS6	PSD8	PLS62-W
V_O	1.80V +1% -5%	1.80V ±3%			
V_O Power save mode		1.80V ±5%			
$I_O$max	-50mA	-10mA			
$I_O$max Power save mode		-10mA			
$C_L$max	1µF	100nF			

3.2.5 Power Indication

All modules support a power indication signal, which is driven by on open collector output. An external pull-up resistor is required.

Table 6: Power indication signal

PWR_IND	PLS8	PDS5	PDS6	PSD8	PLS62-W
V_{IH}max	5.5V	5.5V	5.5V	5.5V	5.5V
V_{OL}max	0.4V at 1mA	0.4V at 2mA	0.4V at 2mA	0.4V at 2mA	0.4V at 2mA
Module ON	low	low	low	low	low

3.2.6 RTC Backup VDDLP

The power supply pad VDDLP can be used to backup the internal RTC from an external capacitor.

Table 7: RTC Backup VDDLP

VDDLP	PLS8	PDS5	PDS6	PSD8	PLS62-W
V_I	Not supported	1.0V … 1.9V at I_{typ} < 1µA			
V_O		1.8V (typ) $I_o$max = -25mA			

3.2.7 Power Supply Ratings

Power supply ratings differ between PHS8 and PDSx, and are listed in the following Table 8.

Reference:

- “Hardware Interface Description”: Section “Power Supply Ratings”

Table 8: Power supply ratings

	Description	Conditions	PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
BATT+	Supply voltage Voltage must stay within the min/max values, including voltage drop, ripple, spikes	Directly measured at Module.	3.3	3.8	4.2	3.3		4.5	3.3		4.5	3.0	3.8	4.5	V
	Maximum allowed voltage drop during transmit burst	Normal condition, power control level for Pout max			400			400			400			400	mV
	Voltage ripple	Normal condition, power control level for Pout max													
		@ f <= 250 kHz			120			190			190			120	mVpp
		@ f > 250 kHz			90			30			30			90	mVpp
I_{VDDLP} @ 3V[1)]	OFF State supply current	RTC backup @ BATT+ = 0V	---				2.0			2.0			1.0		µA
I_{BATT+} [2)]	OFF State supply current	Power Down		40			60			60			TBD.		µA
	Average GSM / GPRS supply current (GNSS off)	SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=9		2.0			0.9 / 1.1			0.9 / 1.1			TBD.		mA
		SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=5		2.5			1.1 / 1.3			1.1 / 1.3			TBD.		mA
		SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=2		3.7			1.4 / 1.6			1.4 / 1.6			3.0/ 3.5		mA
		IDLE[4)] (USB disconnected, UART active) @ DRX=2		75			14			14			14		mA
		IDLE[4)] (USB active) @ DRX=2		90			36			36			33		mA
		Voice Call GSM850/900; PCL=5		330			245			245		---			mA

[1] PLS62: I_{VDDLP} @ 1.8V

[2] With an impedance of Z_{LOAD}=50Ω at the antenna connector.

[3] Measurements start 6 minutes after switching ON the module, averaging times: SLEEP mode - 3 minutes, transfer modes - 1.5 minutes Communication tester settings: no neighbor cells, no cell reselection etc., RMC (reference measurement channel).

[4] The power save mode is disabled via AT command.

	Description	Conditions		PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		GPRS Data transfer GSM850/900; PCL=5; 1Tx/4Rx	ROPR= max. reduction		320			240			240			255 / 235		mA
			ROPR= no reduction		320			240			240			250 / 240		mA
		GPRS Data transfer GSM850/900; PCL=5; 2Tx/3Rx	ROPR= max. reduction		430			310			310			370 / 345		mA
			ROPR= no reduction		540			430			430			475 / 440		mA
		GPRS Data transfer GSM850/900; PCL=5; 4Tx/1Rx	ROPR= max. reduction		600			330			330			500 / 470		mA
			ROPR= no reduction		930	990[5)]		790			790			900 / 830		mA
		EDGE Data transfer GSM850/900; PCL=5; 1Tx/4Rx	ROPR= max. reduction		220			170			170			165 / 160		mA
			ROPR= no reduction		220			170			170			165 / 160		mA
		EDGE Data transfer GSM850/900; PCL=5; 2Tx/3Rx	ROPR= max. reduction		300			230			230			240 / 230		mA
			ROPR= no reduction		340			295			295			245 / 280		mA
		EDGE Data transfer GSM850/900; PCL=5; 4Tx/1Rx	ROPR= max. reduction		490			360			360			335 / 325		mA
			ROPR= no reduction		570			515			515			530 / 500		mA
		Voice Call GSM1800/1900; PCL=0			240			180			180			---		mA
		GPRS Data transfer GSM1800/1900; PCL=0; 1Tx/4Rx	ROPR= max. reduction		230			180			180			165 / 175		mA
			ROPR= no reduction		230			180			180			165 / 175		mA
		GPRS Data transfer GSM1800/1900; PCL=0; 2Tx/3Rx	ROPR= max. reduction		300			200			200			225 / 235		mA
			ROPR= no reduction		360			310			310			300 / 320		mA
		GPRS Data transfer GSM1800/1900; PCL=0; 4Tx/1Rx	ROPR= max. reduction		410			240			240			300 / 315		mA
			ROPR= no reduction		590			550			550			530 / 565		mA

[5)] At total mismatch

	Description	Conditions		PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		EDGE Data transfer GSM1800/1900; PCL=0; 1Tx/4Rx	ROPR= max. reduction		190			150			150			130 / 135		mA
			ROPR= no reduction		190			150			150			130 / 135		mA
		EDGE Data transfer GSM1800/1900; PCL=0; 2Tx/3Rx	ROPR= max. reduction		250			220			220			185 / 190		mA
			ROPR= no reduction		290			250			250			215 / 230		mA
		EDGE Data transfer GSM1800/1900; PCL=0; 4Tx/1Rx	ROPR= max. reduction		380			350			350			255 / 265		mA
			ROPR= no reduction		460			430			430			375 / 400		mA
	Peak current during GSM transmit burst	VOICE Call GSM850/900; PCL=5			2.1	2.4[5)]		1.6	2.3[5)]		1.6	2.3[5)]				A
		VOICE Call GSM1800/1900; PCL=0			1.3	1.6[5)]		1.1	1.4[5)]		1.1	1.4[5)]				A
		GPRS Data transfer GSM850; PCL=5; 4Tx/ 1Rx @ 50Ω												2.2		A
		GPRS Data transfer GSM900; PCL=5; 4Tx/ 1Rx @ 50Ω												2.1		A
		GPRS Data transfer DCS1800; PCL=0; 4Tx/ 1Rx @ 50Ω												1.3		A
		GPRS Data transfer PCS1900; PCL=0; 4Tx/ 1Rx @ 50Ω												1.4		A
	Average GSM / GNSS supply current (GNSS on)	GSM active (UART/USB active); @DRX=2 & GNSS NMEA output off			65		---				55[7]		---			mA
		GSM active (UART/USB active); @DRX=2 & GNSS NMEA output on[6]			85		---				55[7]		---			mA
	Average WCDMA supply current (GNSS off) Data transfers measured @maximum Pout	SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=9			1.8			1.2 / 1.4			1.3			TBD.		mA
		SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=8			2.1			1.2 / 1.4			1.5			TBD.		mA
		SLEEP[3)] (USB Suspend or USB disconnected and no communication via ASC0) @ DRX=6			3.3			1.8 / 2.0			2.1 / 2.0			3.3 / 3.4		mA

[6] One fix per second.

	Description	Conditions	PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		IDLE[4] (USB disconnected, UART active) @ DRX=6		50			13			16			13.8		mA
		IDLE[4] (USB active) @ DRX=6		65			35			35			32.6		mA
		Voice Call Band I		540			520			565			---		mA
		Voice Call Band I		580	700[5]		560			645			---		mA
		Voice Call Band II		600	780[5]		---			---			---		
		Voice Call Band IV		490			---			---			---		mA
		Voice Call Band V/VI		470			460			650			---		mA
		Voice Call Band VIII		640			530			650			---		mA
		UMTS Data transfer Band I		560			440			585			730		mA
		UMTS Data transfer Band II		580			490			640			600		mA
		UMTS Data transfer Band III		620			---			---			---		
		UMTS Data transfer Band IV		520			---			---			560		mA
		UMTS Data transfer Band V/VI		490			410			645			570		mA
		UMTS Data transfer Band VIII		500			470			645			550		mA
		UMTS Data transfer Band IX		---			---			---			655		mA
		UMTS Data transfer Band XIX		---			---			---			600		mA
		HSPA Data transfer Band I		590			440			515			750		mA
		HSPA Data transfer Band II		590			490			590			605		mA
		HSPA Data transfer Band III		620			---			---					mA
		HSPA Data transfer Band IV		540			---			---			560		mA
		HSPA Data transfer Band V/VI		510			410			595			570		mA
		HSPA Data transfer Band VIII		510			470			605			545		mA
		HSPA Data transfer Band IX		---			---			---			660		mA
		HSPA Data transfer Band XIX		---			---			---			610		mA
	Average WCDMA/ GNSS supply current	WCDMA active (UART / USB active); @DRX=6 & GNSS NMEA output off		65			---			55[7]			---		mA

[7] Only for PDS8 with DRX=6

	Description	Conditions		PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	(GNSS on)	WCDMA active (UART / USB active); @DRX=6 & GNSS NMEA output on [6]			85			---			55[7]			---		mA
	Average LTE supply current[8] (GNSS off) Data transfers measured @maximum Pout	SLEEP[3] @ "Paging Occasions" = 256	USB disconnected		2.3			---			---			TBD.		mA
		SLEEP[3] @ "Paging Occasions" = 128	USB disconnected		2.7			---			---			3.2		mA
		SLEEP[3] @ "Paging Occasions" = 64	USB disconnected		3.5			---			---			4.2		mA
		SLEEP[3] @ "Paging Occasions" = 32	USB disconnected		5.4			---			---			5.6		mA
		IDLE	USB disconnected		35			---			---			16		mA
			USB active		45			---			---			35.5		mA
		LTE Data transfer Band 1			---			---			---			825		mA
		LTE Data transfer Band 2			620	740[5]		---			---			685		mA
		LTE Data transfer Band 3			650	830[5]		---			---			650		mA
		LTE Data transfer Band 4			540			---			---			640		mA
		LTE Data transfer Band 5			550			---			---			710		mA
		LTE Data transfer Band 7			640			---			---			685		mA
		LTE Data transfer Band 8			520			---			---			590		mA
		LTE Data transfer Band 12			---			---			---			585		mA
		LTE Data transfer Band 13			570			---			---			---		mA
		LTE Data transfer Band 17			550			---			---			---		mA
		LTE Data transfer Band 18			---			---			---			705		mA
		LTE Data transfer Band 19			---			---			---			665		mA
		LTE Data transfer Band 20			520			---			---			525		mA
		LTE Data transfer Band 28			---			---			---			590		mA

[8] Communication tester settings: - Channel Bandwidth: 5MHz, - Number of Resource Blocks: 25 (DL), 1 (UL), - Modulation: QPSK

	Description	Conditions	PLS8			PDS5			PDS6/PDS8			PLS62-W			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Average LTE supply current (GNSS on)	LTE active (UART / USB active); @DRX=6 & GNSS NMEA output off		65			---			---			---		mA
		LTE active (UART / USB active); @DRX=6 & GNSS NMEA output on [6)]		85			---			---			---		mA

3.2.8 SIM Interface

All modules have no internal ESD protection implemented. Therefore, it is recommended to implement an additional ESD protection close to the SIM card holder. An example is shown in Figure 3. PLS8 and PLS62-W provide two SIM Interfaces.

CCIO line requires on all modules no external pull-up resistor.

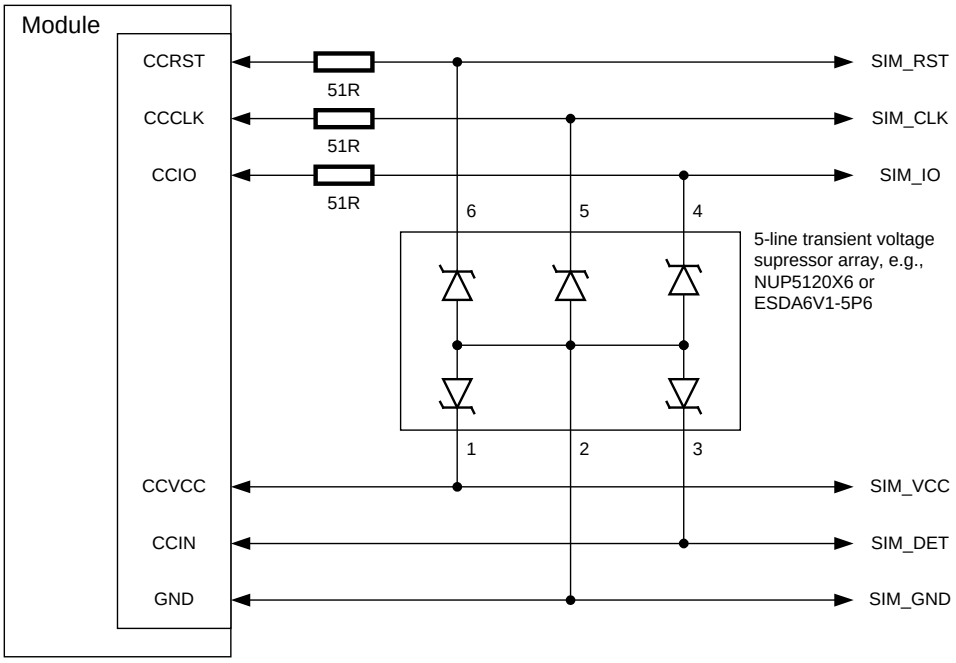


Figure 3: SIM interface - enhanced ESD protection

Reference:

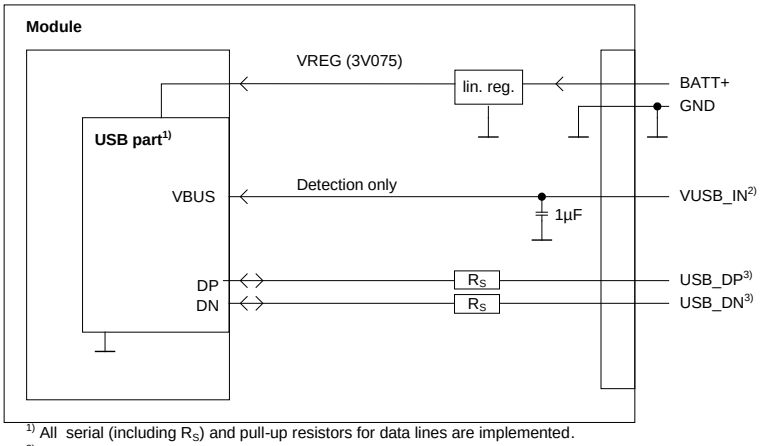
- “Hardware Interface Description”: Section “SIM Interface”

3.2.9 USB Interface

All modules support a USB 2.0 High Speed (480Mbps) device interface that is Full Speed (12Mbps) compliant. The USB interface is primarily intended for use as command and data interface and for downloading firmware.

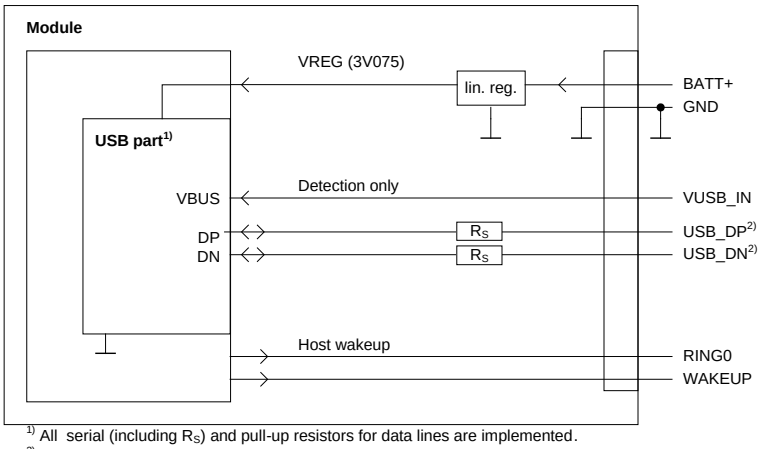
The external application is responsible for supplying the VUSB_IN line. This line is used for cable detection only. The USB part (driver and transceiver) is supplied by means of BATT+. This is because these modules are designed as a self-powered device compliant with the "Universal Serial Bus Specification Revision 2.0".

An external ESD protection should be provided for the USB interfaces.



1) All serial (including R_S) and pull-up resistors for data lines are implemented.
2) Since VUSB_IN is used for detection only it is recommended not to add any further blocking capacitors on the VUSB_IN line.
3) If the USB interface is operated in High Speed mode (480MHz), it is recommended to take special care routing the data lines USB_DP and USB_DN. Application layout should in this case implement a differential impedance of 90Ohm for proper signal integrity.

Figure 4: USB circuit on PLS8



1) All serial (including R_S) and pull-up resistors for data lines are implemented.
2) If the USB interface is operated in High Speed mode (480MHz), it is recommended to take special care routing the data lines USB_DP and USB_DN. Application layout should in this case implement a differential impedance of 90 ohms for proper signal integrity.

Figure 5: USB circuit on PDS5/6/8 and PLS62-W

Reference:

- "Hardware Interface Description": Section "USB Interface"

3.2.10 ASC0 Interface

The voltage levels at the ASC0 interface lines are identical for all. The following tables show ASC0 interface differences between the modules.

Table 9: ASC0 transfer rates

ASC0	PLS8	PDS5	PDS6/PDS8	PLS62-W
Baud rate range	115200bps	1200 … 921600bps		
Autobauding	Not supported	1200 … 230400 bps		
Flow Control	RTS/CTS	RTS/CTS		

Table 10: ASC0 signals at reset/start-up/operation[10]

ASC0 interface lines	PLS8	PDS5	PDS6/PDS8	PLS62-W
RXD0	PD / PU / PU	PU / PU / O,H	PU / PU / O,H	PU / O,H / O,H
TXD0	PD / PD / PD	PD / PD / I	PD / PD / I	PD / I / I
CTS0	PD / PD / PD	PU / PU / O,H	PU / PU / O,H	PU / O,H / O,H
RTS0	PU & PD / PD / PD	PU / PU / I, PD	PU / PU / I,PD	PU / I,PD / I,PD
DTR0	PD / PD / PD	PD / PD / I	PD / PD / I	PD / PD / I
DCD0	PD / PU / PD	PD / PU / O,H	PD / PU / O,H	PD / PD / O,H
DSR0	PD / PD / PD	PD / PU / O,L	PD / PU / O,L	PD / PD / O,L
RING0	PD / PD / O,H	PD / PU / O,H	PD / PU / O,H	PD / PD / O,H

For more information on the interface and its start-up timings please refer to the specific “Hardware Interface Description”.

[10] PU = Pull-up (~100kΩ); PD = Pull-down (~100kΩ); I = Input; O = Output; L = low; H = High

3.2.11 Digital Audio Interface

PLS8, PDS5, PDS6 and PDS8 support a pulse code modulation (PCM) interface. PLS62-W currently support no digital audio interface, but the HW is prepared.

The PCM interface can be enabled using the AT command AT^SAIC.

Table 11: PCM characteristics

PCM interface	PLS8	PDS5	PDS6/PDS8	PLS62-W
Mode	Master / Slave	Master	Master	Not supported, HW prepared
Clock [kHz]	128 (Master only), 256, 1024, 2048	256	256	
Sync	Short, Long (128kHz)	Long	Long	
Sampling rate	8 and 16 kHz	8 kHz	8 kHz	

There are no differences, when the PCM interface is inactive.

Table 12: PCM inactive signal states[11]

PCM interface	PLS8	PDS5	PDS6/PDS8	PLS62-W[12]
PCM_OUT	PD	PD	PD	PD
PCM_IN	PD	PD	PD	PD
PCM_FSC	PD	PD	PD	PD
PCM_CLK	PD	PD	PD	PD

For more information on the interface and its start-up timings please refer to the specific “Hardware Interface Description”.

[11] PU = Pull-up (~100kΩ); PD = Pull-down (~100kΩ)
[12] shared with GPIO

3.2.12 Inter IC Sound Interface (I^2S)

PLS8 supports an inter IC sound interface.

The I^2S interface can be enabled using the AT command AT^SAIC. Activation is possible only out of call and out of tone presentation. The I^2S properties and capabilities comply with the requirements layed out in the Phillips I^2S Bus Specifications, revised June 5, 1996.
The I^2S Interface is a dual interface that provides possibility to transfer mono as well as dual/stereo audio signals in either direction.

Table 13: I^2S Interface capabilities

I^2S interface	**PLS8**	**PDS5**	**PDS6/PDS8**	**PLS62-W**
Mode	Master	Not supported	Not supported	Not supported
Interface lines	5			
Sampling rate	8 or 16 kHz			
Coding	16 bit linear			
Uplink channel	Left			
Downlink Channel	Left			
Dual Microphone for non-stationary background noise suppression	No			

Table 14: I^2S inactive signal states[13]

I2S interface	**PCM interface**	**PLS8**	**PDS5**	**PDS6/PDS8**	**PLS62-W[14]**
I2S_DOUT	PCM_OUT	PD	PD	PD	PD
I2S_DIN	PCM_IN	PD	PD	PD	PD
I2S_WS	PCM_FSC	PD	PD	PD	PD
I2S_SCLK	PCM_CLK	PD	PD	PD	PD
I2S_MCLKOUT		PD	PD	PD	PD

For more information on the interface and its start-up timings please refer to the specific “Hardware Interface Description”.

[13] PU = Pull-up (~100kΩ); PD = Pull-down (~100kΩ)
[14] shared with GPIO

3.2.13 Analogue Audio Interface

For PDS6 an analogue audio interface is implemented.

Table 15: Analogue audio interface

Analogue Audio interface	**PLS8[15]**	**PDS5/PDS8[15]**	**PDS6**	**PLS62-W[15]**
Supported	No	No	Yes	No
VMIC			$V_o$typ = 2.7V±5.5% I_{max} = 3 mA	
MICP1 MICN1			$Z_I$typ = 94k @ 0dB gain $Z_I$typ = 5.8k @ 30dB gain V_{in}max = 0.7V_{RMS} (2.0Vpp)	
Analogue Ground			AGND	
EPP1 EPN1			Differential, Minimum load resistance 16Ω typ. 5.0Vpp at 16Ω load $C_L$max <= 100pF to AGND at each pin.	

[15] In case of supporting analogue audio interface in future releases of PLS8, PDS5, PDS8 and PLS62-W, the same PADs as defined for PDS6 will be used.

3.2.14 GPIO Interface

PLS8 supports 10 GPIOs, one of them is shared with Low Current Indicator
PDS5, PDS6 and PDS8 support 8 GPIOs, some of them shared with Host Wakeup, Fast Shutdown, PWM and Pulse Counter.
PLS62-W supports 24 GPIOs, some of them shared with Fast Shutdown, PWM and Pulse Counter, SPI and second serial interface.

Table 16: GPIO lines (the grey shaded signals have no GPIO functionality, shown only for reference)

PAD	PLS8	PDS5	PDS6/PDS8	PLS62-W
J14	GPIO1	n.a.	n.a.	GPIO15
J15	GPIO2	GPIO2	GPIO2	GPIO14
J16	GPIO3	n.a.	n.a.	GPIO13
H14	GPIO4	GPIO4 / Host Wakeup / Fast Shutdown	GPIO4 / Host Wakeup / Fast Shutdown	GPIO4 / Fast Shutdown
H15	GPIO5	GPIO5	GPIO5	GPIO12
H16	GPIO6 / Low Current Indicator	GPIO6 / PWM2	GPIO6 / PWM2	GPIO6 / PWM2
G14	GPIO7	GPIO7 / PWM1	GPIO7 / PWM1	GPIO7 / PWM1
G15	GPIO8	GPIO8 / Pulse Counter	GPIO8 / Pulse Counter	GPIO8 / Pulse Counter
G16	GPIO9	GPIO9	GPIO9	GPIO11
F16	GPIO10	GPIO10	GPIO10	GPIO25
P6	I2S_MCLKOUT	SPI_MOSI	SPI_MOSI	GPIO16 / RXD1 / SPI_MOSI
P7	rfu(dnu)	SPI_MISO	SPI_MISO	GPIO17 / TXD1 / SPI_MISO
P8	DTR0	DTR0	DTR0	DTR0 / GPIO1
P9	DSR0	DSR0	DSR0	DSR0 / GPIO3 / SPI_CLK
P10	RING0	RING0	RING0	RING0 / GPIO24
N6	rfu(dnu)	SPI_CS	SPI_CS	GPIO19 / CTS1 / SPI_CS
N7	rfu(dnu)	SPI_CLK	SPI_CLK	GPIO18 / RTS1
N9	DCD0	DCD0	DCD0	DCD0 / GPIO2
M7	PCM_I2S_IN	PCM_IN	PCM_IN	GPIO21
M8	PCM_I2S_CLK	PCM_CLK	PCM_CLK	GPIO23
M9	PCM_I2S_FSC	PCM_FSC	PCM_FSC	GPIO22
M10	PCM_I2S_OUT	PCM_OUT	PCM_OUT	GPIO20
L11	rfu(dnu)	rfu(nc)	rfu(nc)	SIM_SWITCH / GPIO26
B14	STATUS	STATUS	STATUS	GPIO5 / STATUS

Table 17: GPIO start-up/reset signal states[16]

GPIO line	PLS8	PDS5	PDS6/PDS8	PLS62-W
J14	PD / PD	PD / PD	PD / PD	PD / PD
J15	PD / PD	PD / PD	PD / PD	PD / PD
J16	PD / PD	PD / PD	PD / PD	PD / PD
H14	PD / PD	PD / PD	PD / PD	PD / PD
H15	PD / PD	PD / PD	PD / PD	PD / PD
H16	PD / PD	PD / PD	PD / PD	L / PD
G14	PD / PD	PD / PD	PD / PD	PD / PD
G15	PD / PD[17]	PD / PD	PD / PD	PD / PD
G16	PD / PD	PD / PD	PD / PD	PD / PD
F16	PD / PD	PD / PD	PD / PD	PD / PD
P6	PD / PD	PD / PD	PD / PD	PU / PD
P7	rfu(dnu)	PD / PD	PD / PD	PD / PD
P8	PD / PD	PD / I	PD / I	PD / PD
P9	PD / PD	PD / O,L	PD / O,L	PD / PD
P10	PD / O,H	PD / O,H	PD / O,H	PD / PD
N6	rfu(dnu)	PD / O,H	PD / O,H	PD / PD
N7	rfu(dnu)	PD / O,H	PD / O,H	PD / PD
N9	PD / PD	PD / O,H	PD / O,H	PD / PD
M7	PU / PD	PD / PD	PD / PD	PD / PD
M8	PD / PD	PD / PD	PD / PD	PD / PD
M9	PD / PD	PD / PD	PD / PD	PD / PD
M10	PD / PD	PD / PD	PD / PD	PD / PD
L11	rfu(dnu)	rfu(nc)	rfu(nc)	PD / PD
B14	PD / PD	PD / O,L	PD / O,L	PD / PD

For more information on the interface and its start-up timings please refer to the specific “Hardware Interface Description”.

[16] PU = Pull-up (~100kΩ); PD = Pull-down (~100kΩ)
[17] During startup phase the GPIO8 signal will be in an active low state for appr. 80ms.

3.2.15 I²C Interface

All PDSx and PLS62-W modules support an I²C interface controlled by the AT^SSPI command. It consists of two lines, the serial data line I²CDAT and the serial clock line I²CCLK. The module acts as a single master device, e.g. the clock I²CCLK is driven by the module. I²CDAT is a bidirectional line.
PLS8 has no I²C interface.

Table 18: I²C characteristics

I²C	PLS8	PDS5	PDS6/PDS8	PLS62-W
Internal pull up resistors	Not supported	2.2kΩ	2.2kΩ	1kΩ
V_{OL}		0.3V @Imax = 4mA	0.3V @Imax = 4mA	0.35V @Imax = 4mA
V_{OH}		1.85V	1.85V	1.85V
V_{IL}max		0.3V	0.3V	0.35V
V_{IH}min		1.35V	1.35V	1.30V
V_{IH}max		1.85V	1.85V	1.85V
Data transfer rate		100kbps/400kbps	100kbps/400kbps	100kbps/400kbps
Mode		Master	Master	Master

For more information on the interface and its start-up timings please refer to the specific "Hardware Interface Description".

3.2.16 SPI Interface

All PDSx and PLS62-W modules support an SPI interface controlled by the AT^SSPI command. The SPI interface comprises the two data lines SPI_MOSI and SPI_MISO, the clock line SPI_CLK as well as the chip select line SPI_CS. The SPI interface supports only master mode. The SPI interface on PLS62-W is shared with GPIO lines.
PLS8 has no SPI interface.

Table 19: SPI characteristics

SPI	PLS8	PDS5	PDS6/PDS8	PLS62-W
V_{OL}max	Not supported	0.25V @ I = 1mA	0.25V @ I = 1mA	0.25V @ I = 1mA
V_{OH}min		1.55V @ I = -1mA	1.55V @ I = -1mA	1.55V @ I = -1mA
V_{OH}max		1.85V	1.85V	1.85V
V_{IL}max		0.35V	0.35V	0.35V
V_{IH}min		1.30V	1.30V	1.30V
V_{IH}max		1.85V	1.85V	1.85V
Data transfer rate		100, 250, 500, 1083, 3.250, 6.500 kbps	100, 250, 500, 1083, 3.250, 6.500 kbps	100, 250, 500, 1083, 3.250, 6.500 kbps
Mode		Master	Master	Master

For more information on the interface and its start-up timings please refer to the specific "Hardware Interface Description".

3.2.17 ADC

All PDSx and PLS62-W modules support one analog-to-digital converter controlled by the AT^SRADC command.
PLS8 provides 3 ADC.

Table 20: ADC characteristics

ADC	PLS8	PDS5	PDS6/PDS8	PLS62-W
Number of ADC	3	1	1	1
Result solution	12 Bit	10 Bit	10Bit	10 Bit
R_I	R_i=1MOhm	R_i=1MOhm	R_i=1MOhm	R_i=1MOhm
Full specification compliance range	$0.3V \le V_I \le 3.075V$	$0V \le V_I \le 1.2V$	$0V \le V_I \le 1.2V$	$0V \le V_I \le 1.2V$
V_{Imax}	3.075V	1.2V	1.2V	1.2V
Analog bandwidth	<16kHz	<16kHz	<16kHz	<16kHz
Integral linearity error	±4 LSB	±2 LSB	±2 LSB	±2 LSB
Offset error	±4 LSB	±1 LSB	±1 LSB	±1 LSB

For more information on the ADC lines please refer to the specific “Hardware Interface Description”.

3.2.18 Network Connectivity Indicator

The STATUS line serves to indicate the module’s network connectivity state and can be used to control an externally connected LED. To operate the LED a buffer, e.g. a transistor or gate, must be included in the external application. On PLS62-W the STATUS line is shared with GPIO.

Table 21: Connectivity and technology indicator characteristics

Connectivity and technology indicator	PLS8	PDS5	PDS6/PDS8	PLS62-W
Connectivity Status	Yes, AT^SLED=1 or 2	Yes, AT^SLED=1 or 2	Yes, AT^SLED=1 or 2	Yes, AT^SLED=1 or 2
Technology Status	Yes, AT^SLED=3	No	No	No
V_{OL}max	0.45V @ 2mA	0.25V @ 1mA	0.25V @ 1mA	0.25V @ 1mA
V_{OH}min	1.35V @ -2mA	1.55V @ -1mA	1.55V @ -1mA	1.55V @ -1mA
V_{OH}max	1.85V	1.85V	1.85V	1.85V

The AT command AT^SLED and the state indications are described in the AT Command Specification of the module.

3.3 Antenna Interface

3.3.1 RF Antenna

The PLS8 and PLS62-W antenna interfaces have no internal ESD protection implemented. Therefore, especially if the antenna interfaces are accessible to the end user of the final product, it is recommended to add an external ESD protection. An example of an additional ESD external protection circuit is given in Figure 6. The additional components should be placed as close as possible to the antenna pad.

The PDS5, PDS6, and PDS8 antenna interfaces have an internal ESD protection implemented. For compatibility reasons and a possible migration to PLS8 or PLS62-W however, it is advised to envisage the recommended possible ESD protection circuits (T pad or PI pad) in external applications currently using PHS8 and AHS modules (see Figure 7). The placement options may then later be activated if required.

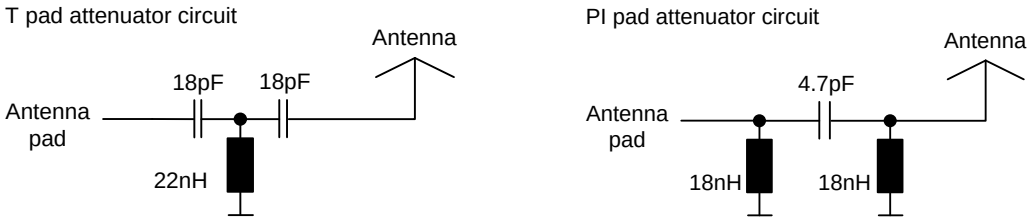


Figure 6: Possible PLS8 and ALS3 ESD protection circuits - T or PI pad

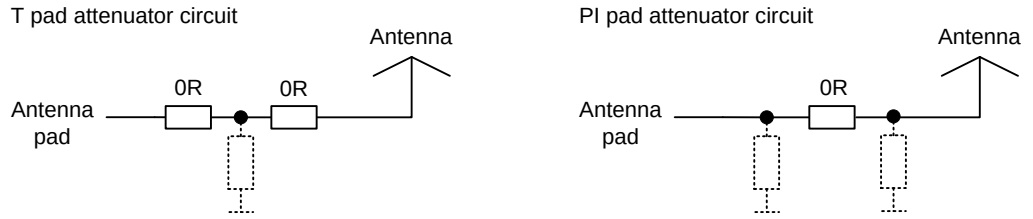


Figure 7: Possible designated ESD protection circuit - T or PI pad

Table 22: ESD protection on external application

RF antenna	PDS5/PDS6/PDS8	PLS8 and PLS62-W
Internal ESD protection	Supported	Not supported
22nH inductor placement (T pad) or 18nH inductors placement (PI pad)	No	Yes (Recommended inductor type: Size 0402 SMD from Panasonic ELJRF series (22nH and 18nH inductors) or Murata LQW15AN18NJ00 (18nH inductors only)
Value of serial capacitors (T pad) or Value of serial capacitor (PI pad)	0 Ohm 0 Ohm	18pF 4.7pF

For more information on the RF antenna interface please refer to the specific “Hardware Interface Description”.

3.3.2 GNSS Antenna

PLS8 and PDS8 support GNSS with external active and passive antenna. PLS8 supports GPS and GLONASS, PDS8 only GPS.

The modules provide a power supply for active antenna, which is controlled by AT Command.

Table 23: Supply voltage for active GNSS antenna

	PLS8	**PDS5/PDS6**	**PDS8**	**PLS62-W**
VGNSS (Output)	$C_L$max = 2.2µ; V_O = 3.05V ±1% @I_O = -20mA; $I_O$max = -50mA	Not supported	$C_L$max = 2.2µ; V_O = 3.05V ±1% @I_O = -20mA; $I_O$max = -50mA	Not supported
ANT_GNSS_DC (input)	$V_I$max = 6V The input current has to be limited at 50mA (antenna short circuit protection)	Not supported	$V_I$max = 6V The input current has to be limited at 50mA (antenna short circuit protection)	Not supported

For more information on the GNSS antenna interface please refer to the specific “Hardware Interface Description”.

4 Common Footprint Design

The following chapter shows the pad assignment differences between all Gemalto M2M modules described in this document. It notes the modifications a possible common footprint design will have to allow for in order to provide an easy migration path from one product to the next one.

The following figures show that only few changes are required to adapt an existing hardware platform to meet the requirements of another product.

When using the same footprint for different products take care that the following requirements be met:

- Pads marked grey and labeled “rfu (dnu)”, “rfu (GND)” or “rfu (nc)” must be left unconnected, but can be soldered.
- Pads marked orange and labeled “BATT+RF” can still be connected and soldered when using the PLS8 or PLS62-W, because these modules use only one power domain named “BATT+RF” for all supported wireless technologies.
- Pads marked gold are related to the analogue audio interface. When analogue audio is not supported by the module, then these pads are not connected inside the module (nc). The pad C15 (AGND) can be always connected to GND.
- Pads marked olive are related to GPIOs and should be only connected when used, but can be soldered. PLS62-W will have a different numbering of some of these GPIOs.
- Pads marked lime-green are related to second SIM interface. These pads should be only connected when used, but can be soldered.
- Pad marked pink and labeled “ADCx_IN” should be only connected when used, but can be soldered.
- Pad marked yellow and labeled “VDDLP can still be connected and soldered as long as the input voltage does not exceed the limit of the used module.
- Pads marked violet can be soldered and connected when needed. PLS8 provides one signal for I2S interface. PDS5/6/8 supports on these Pads an SPI interface. PLS62-W provides on this lines GPIOs shared with ASC1 and data lines of the SPI interface
- Pads marked brown and labeled “ANT_GNSS” or “ANT_GPS”, “VGNSS” or “VGPS” and “ANT_GNSS_DC” or ANT_GPS_DC can be soldered and connected. Only PLS8 and PDS8 support GNSS/GPS functionality. On PDS5, PDS6 and PLS62-W these pads are not connected internally.
- Pads marked with light blue are used for special functions, which are only supported by PLS62-W. These pads can be soldered and connected when needed.

“nc” indicates a pad that is electrically not connected on the module. This means that in a common footprint only the other functionality may be implemented for the appropriate module without having to take a transition from one assignment to another into account.

Table 24: Pad to signal comparison

Pad No.	Signal name				
	PLS8	PDS5	PDS6	PDS8	PLS62-W
A4	nc	BATT+RF	BATT+RF	BATT+RF	nc
A5	GND	GND	GND	GND	GND
A6	GND	GND	GND	GND	GND
A7	rfu (dnu)	rfu (GND)	rfu (GND)	rfu (GND)	rfu (GND)
A8	GND	GND	GND	GND	GND
A9	GND	rfu (dnu)	rfu (dnu)	rfu (dnu)	GND
A10	GND	GND	GND	GND	GND
A11	GND	GND	GND	GND	GND
A12	ANT_DRX_MIMO	rfu (nc)	rfu (nc)	rfu (nc)	ANT_DRX
A13	GND	GND	GND	GND	GND
B3	nc	BATT+RF	BATT+RF	BATT+RF	nc
B4	GND	GND	GND	GND	GND
B5	GND	GND	GND	GND	GND
B6	GND	GND	GND	GND	GND
B7	GND	GND	GND	GND	GND
B8	GND	GND	GND	GND	GND
B9	GND	GND	GND	GND	GND
B10	GND	GND	GND	GND	GND
B11	GND	GND	GND	GND	GND
B12	GND	GND	GND	GND	GND
B13	GND	GND	GND	GND	GND
B14	STATUS	STATUS	STATUS	STATUS	STATUS/GPIO5
C2	GND	GND	GND	GND	GND
C3	GND	GND	GND	GND	GND
C4	GND	GND	GND	GND	GND
C5	GND	GND	GND	GND	GND
C6	GND	GND	GND	GND	GND
C7	GND	GND	GND	GND	GND
C8	GND	GND	GND	GND	GND
C9	GND	GND	GND	GND	GND
C10	GND	GND	GND	GND	GND
C11	GND	GND	GND	GND	GND
C12	rfu (GND)	rfu (GND)	rfu (GND)	rfu (GND)	rfu (nc)
C13	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
C14	rfu (nc)	rfu (nc)	VMIC	rfu (nc)	rfu (nc)
C15	rfu (GND)	rfu (GND)	AGND	rfu (GND)	rfu (GND)
D1	GND	GND	GND	GND	GND
D2	GND	GND	GND	GND	GND
D3	GND	GND	GND	GND	GND
D4	GND	GND	GND	GND	GND
D5	ANT_GNSS_DC	rfu (nc)	rfu (nc)	ANT_GPS_DC	rfu (dnu)
D6	GND	GND	GND	GND	GND
D7	GND	GND	GND	GND	GND
D8	GND	GND	GND	GND	GND
D9	GND	GND	GND	GND	GND
D10	GND	GND	GND	GND	GND

Pad No.	Signal name				
	PLS8	PDS5	PDS6	PDS8	PLS62-W
D11	GND	GND	GND	GND	GND
D12	CCIN2	rfu (nc)	rfu (nc)	rfu (nc)	CCIN2
D13	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
D14	CCCLK2	rfu (nc)	rfu (nc)	rfu (nc)	CCCLK2
D15	rfu (nc)	rfu (nc)	MICP	rfu (nc)	rfu (dnu)
D16	rfu (nc)	rfu (nc)	MICN	rfu (nc)	rfu (nc)
E1	ANT_GNSS	rfu (nc)	rfu (nc)	ANT_GPS	rfu (nc)
E2	GND	GND	GND	GND	GND
E3	GND	GND	GND	GND	GND
E4	GND	GND	GND	GND	GND
E5	GND	GND	GND	GND	GND
E12	CCIO2	rfu (nc)	rfu (nc)	rfu (nc)	CCIO2
E13	CCRST2	rfu (nc)	rfu (nc)	rfu (nc)	CCRST2
E14	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
E15	rfu (nc)	rfu (nc)	EPP	rfu (nc)	rfu (nc)
E16	rfu (nc)	rfu (nc)	EPN	rfu (nc)	rfu (nc)
F1	GND	GND	GND	GND	GND
F2	GND	GND	GND	GND	GND
F3	GND	GND	GND	GND	GND
F4	GND	GND	GND	GND	GND
F13	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
F14	rfu (dnu)	I^2CCLK	I^2CCLK	I^2CCLK	I^2CCLK
F15	rfu (dnu)	I^2CDAT	I^2CDAT	I^2CDAT	I^2CDAT
F16	GPIO10	GPIO10	GPIO10	GPIO10	GPIO25
G1	GND	GND	GND	GND	GND
G2	GND	GND	GND	GND	GND
G3	GND	GND	GND	GND	GND
G4	rfu (dnu)	rfu (GND)	rfu (GND)	rfu (GND)	GND
G13	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
G14	GPIO7	GPIO7/ PWM1	GPIO7/ PWM1	GPIO7/ PWM1	GPIO7/ PWM1
G15	GPIO8	GPIO8/ COUNTER	GPIO8/ COUNTER	GPIO8/ COUNTER	GPIO8/ COUNTER
G16	GPIO9	GPIO9	GPIO9	GPIO9	GPIO11
H1	GND	GND	GND	GND	GND
H2	GND	GND	GND	GND	GND
H3	GND	GND	GND	GND	GND
H4	GND	GND	GND	GND	GND
H13	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
H14	GPIO4	GPIO4/ FST_SHDN/ H_WAKEUP	GPIO4/ FST_SHDN/ H_WAKEUP	GPIO4/ FST_SHDN/ H_WAKEUP	GPIO4/ FST_SHDN
H15	GPIO5	GPIO5	GPIO5	GPIO5	GPIO12
H16	GPIO6/ LCI_IND	GPIO6/ PWM2	GPIO6/ PWM2	GPIO6/ PWM2	GPIO6/PWM2
J1	GND	GND	GND	GND	GND
J2	GND	GND	GND	GND	GND
J3	GND	GND	GND	GND	GND

Pad No.	Signal name				
	PLS8	PDS5	PDS6	PDS8	PLS62-W
J4	GND	GND	GND	GND	GND
J13	GND	rfu (GND)	rfu (GND)	rfu (GND)	GND
J14	GPIO1	rfu (fix 100k pull down)	rfu (fix 100k pull down)	rfu (fix 100k pull down)	GPIO15
J15	GPIO2	GPIO2	GPIO2	GPIO2	GPIO14
J16	GPIO3	rfu (fix 100k pull down)	rfu (fix 100k pull down)	rfu (fix 100k pull down)	GPIO13
K1	ANT_MAIN	ANT_GSM	ANT_GSM	ANT_GSM	ANT_MAIN
K2	GND	GND	GND	GND	GND
K3	GND	GND	GND	GND	GND
K4	GND	GND	GND	GND	GND
K5	GND	GND	GND	GND	GND
K12	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
K13	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
K14	CCIO1	CCIO	CCIO	CCIO	CCIO1
K15	CCVCC1	CCVCC	CCVCC	CCVCC	CCVCC1
K16	VGNSS	rfu(nc)	rfu(nc)	VGPS	rfu (nc)
L1	GND	GND	GND	GND	GND
L2	GND	GND	GND	GND	GND
L3	GND	GND	GND	GND	GND
L4	GND	GND	GND	GND	GND
L5	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	TX_ACTIVITY
L6	CCVCC2	rfu (nc)	rfu (nc)	rfu (nc)	CCVCC2
L7	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)
L8	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)
L9	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)
L10	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	ANT_SWITCH
L11	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	SIM_SWITCH/ GPIO26
L12	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
L13	rfu (dnu)	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
L14	CCRST1	CCRST	CCRST	CCRST	CCRST1
L15	CCCLK1	CCRST	CCCLK	CCCLK	CCCLK1
L16	IGT	IGT	IGT	IGT	IGT
M2	GND	GND	GND	GND	GND
M3	GND	GND	GND	GND	GND
M4	PWR_IND	PWR_IND	PWR_IND	PWR_IND	PWR_IND
M5	VEXT	V180	V180	V180	V180
M6	GND	GND	GND	GND	GND
M7	PCM_IN/ I2S_DIN	PCM_IN	PCM_IN	PCM_IN	GPIO21
M8	PCM_CLK/ I2S_SCLKIN	PCM_CLK	PCM_CLK	PCM_CLK	GPIO23
M9	PCM_FSC/ I2S_WSIN	PCM_FSC	PCM_FSC	PCM_FSC	GPIO22
M10	PCM_OUT/ I2S_DOUT	PCM_OUT	PCM_OUT	PCM_OUT	GPIO20
M11	ADC3_IN	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)

Pad No.	Signal name				
	PLS8	PDS5	PDS6	PDS8	PLS62-W
M12	ADC2_IN	rfu (nc)	rfu (nc)	rfu (nc)	rfu (nc)
M13	ADC1_IN	ADC1_IN	ADC1_IN	ADC1_IN	ADC1_IN
M14	CCIN1	CCIN	CCIN	CCIN	CCIN1
M15	VDDLP	VDDLP	VDDLP	VDDLP	VDDLP
N3	BATT+_RF	BATT+RF	BATT+RF	BATT+RF	BATT+RF
N4	BATT+_RF	BATT+RF	BATT+RF	BATT+RF	BATT+RF
N5	VUSB_IN	VUSB_IN	VUSB_IN	VUSB_IN	VUSB_IN
N6	rfu (dnu)	SPI_CS	SPI_CS	SPI_CS	GPIO19/ CTS1/ SPI_CS
N7	rfu (dnu)	SPI_CLK	SPI_CLK	SPI_CLK	GPIO18/ RTS1
N8	CTS0	CTS0	CTS0	CTS0	CTS0
N9	DCD0	DCD0	DCD0	DCD0	DCD0/ GPIO2
N10	RTS0	RTS0	RTS0	RTS0	RTS0
N11	GND	GND	GND	GND	GND
N12	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)	rfu (dnu)
N13	BATT+	BATT+	BATT+	BATT+	BATT+
N14	EMERG_OFF	EMERG_OFF	EMERG_OFF	EMERG_OFF	EMERG_OFF
P4	USB_DP	USB_DP	USB_DP	USB_DP	USB_DP
P5	USB_DN	USB_DN	USB_DN	USB_DN	USB_DN
P6	I2S_MCLKOUT	SPI_MOSI	SPI_MOSI	SPI_MOSI	GPIO16/ RXD1/ SPI_MOSI
P7	rfu (dnu)	SPI_MISO	SPI_MISO	SPI_MISO	GPIO17/ TXD1/ SPI_MISO
P8	DTR0	DTR0	DTR0	DTR0	DTR0/ GPIO1
P9	DSR0	DSR0	DSR0	DSR0	DSR0/ GPIO3/ SPI_CLK
P10	RING0	RING0	RING0	RING0	RING0/ GPIO24
P11	RXD0	RXD0	RXD0	RXD0	RXD0
P12	TXD0	TXD0	TXD0	TXD0	TXD0
P13	BATT+	BATT+	BATT+	BATT+	BATT+

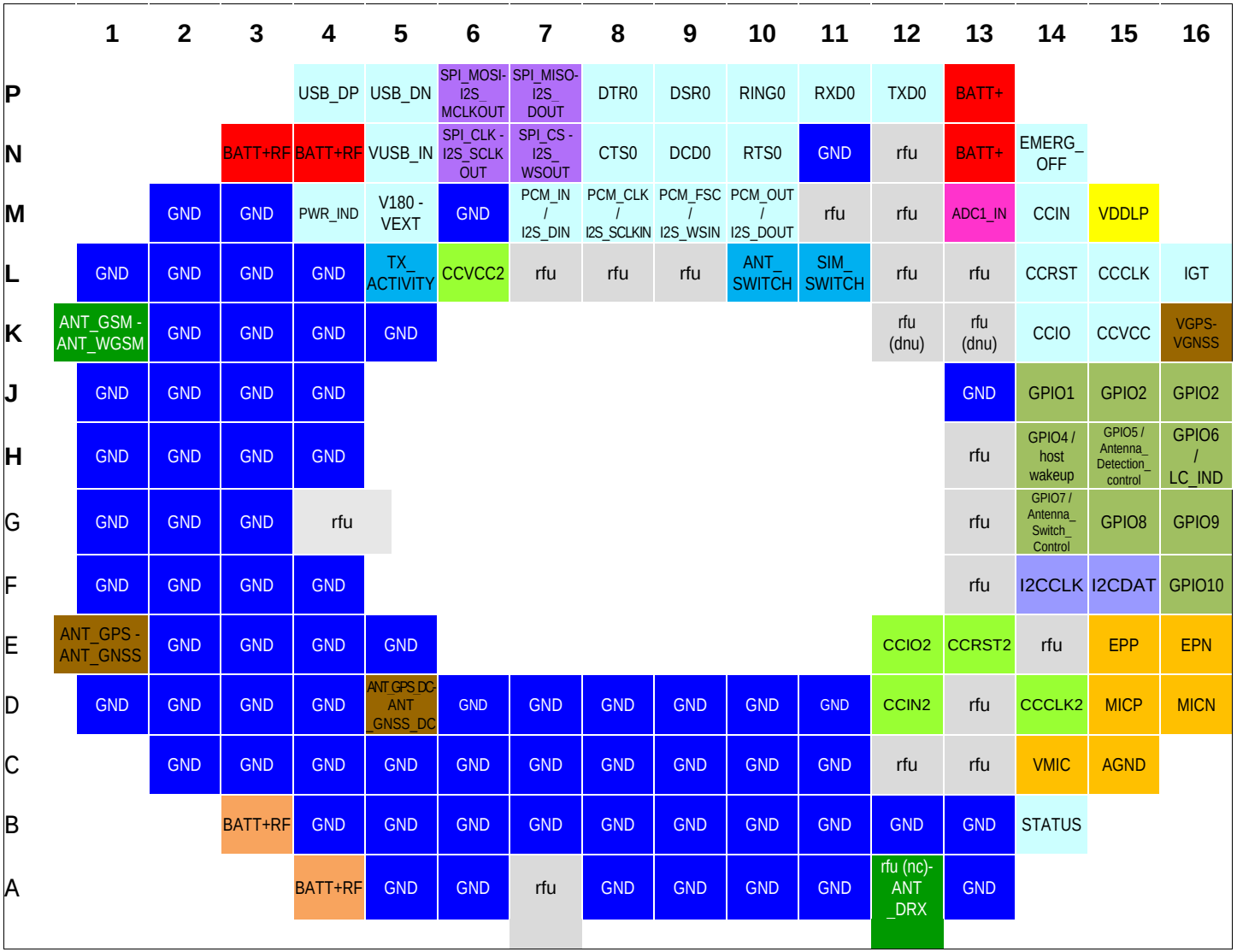


Figure 8: Common footprint

4.1 Common Land Pattern

Figure 6 shows a common land pattern for PHS8, PDS5, PDS6 and PDS8.

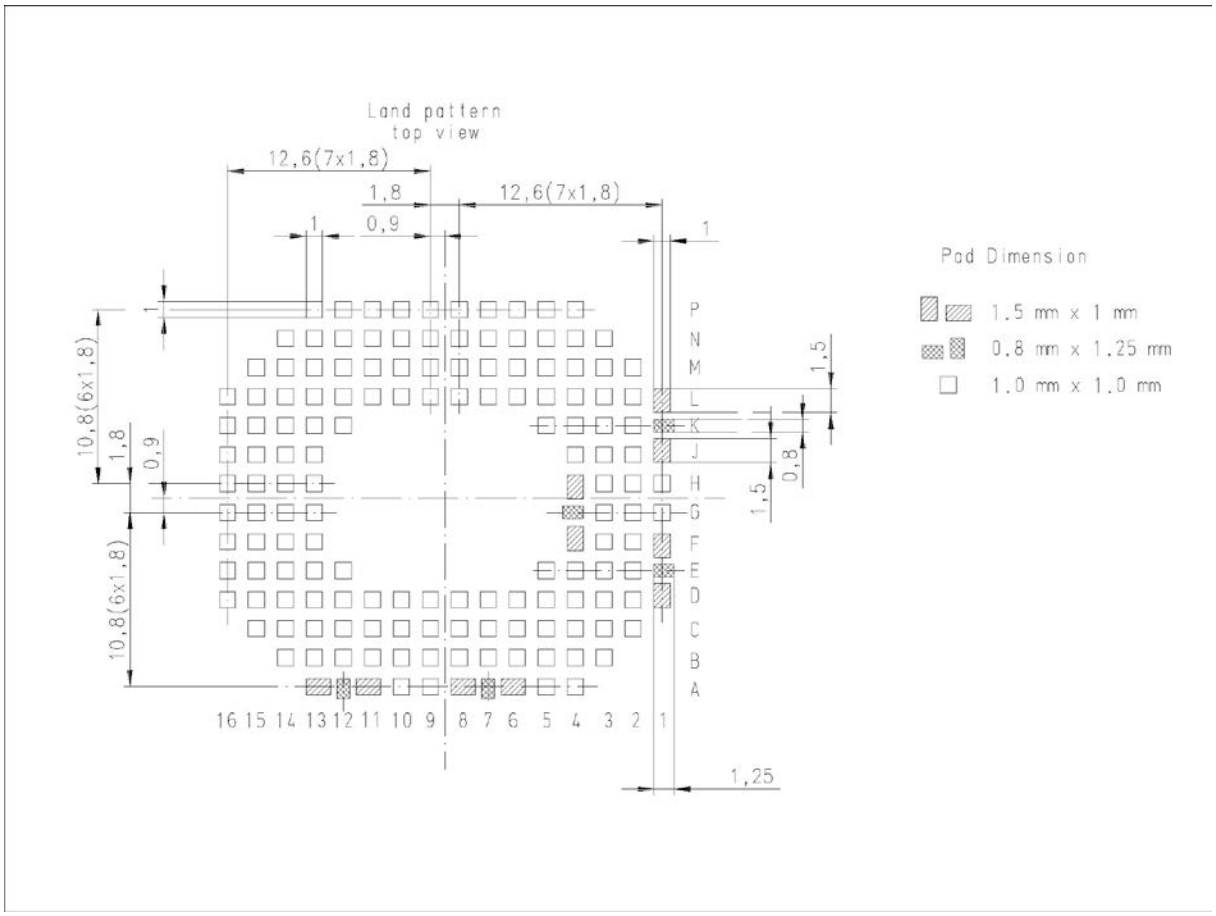


Figure 9: Common land pattern (top view)

About Gemalto

Gemalto (Euronext NL0000400653 GTO) is the world leader in digital security with 2011 annual revenues of €2 billion and more than 10,000 employees operating out of 74 offices and 14 Research & Development centers, located in 43 countries.

We are at the heart of the rapidly evolving digital society. Billions of people worldwide increasingly want the freedom to communicate, travel, shop, bank, entertain and work - anytime, everywhere - in ways that are enjoyable and safe. Gemalto delivers on their expanding needs for personal mobile services, payment security, authenticated cloud access, identity and privacy protection, eHealthcare and eGovernment efficiency, convenient ticketing and dependable machine-to-machine (M2M) applications.

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