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APPLICATION NOTE 5314

Power Sequencing the MAX14885E VGA Crossover Switch

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Abstract: The MAX14885E, a fully integrated low-capacitance VGA dual-graphics crossover switch, connects a VGA source to a VGA monitor. This application note explains the proper sequencing of the MAX14885E's two power supplies, V_{CC} and V_L , on power-up.

Introduction

The [MAX14885E](#), a 2:2 VGA switch, connects a VGA source to a VGA monitor. To ease direct connection to graphics controllers or the ASIC, the MAX14885E has two supplies: V_{CC} , a 5V \pm 5% supply, drives the VGA side interface; and the V_L supply sets the logic switching thresholds on the digital input pins (EN, S00, S01, S10, S11, SHA, SHB, SVA, and SVB). This application note documents the proper sequencing of the V_{CC} and V_L power supplies on power-up.

Proper Power Sequencing

To ensure that the MAX14885E operates correctly, the V_{CC} and V_L supplies must be properly sequenced. It is easiest to understand the correct sequencing conditions if we split the discussion into two cases: first, when V_L rises before (or coincidentally) with V_{CC} ; and second, the case when V_L rises after V_{CC} .

Case 1: When V_L Rises Before V_{CC}

The MAX14885E powers up properly when V_L rises before V_{CC} rises or when it rises coincidentally with V_{CC} . This is shown in **Figures 1** and **2**.

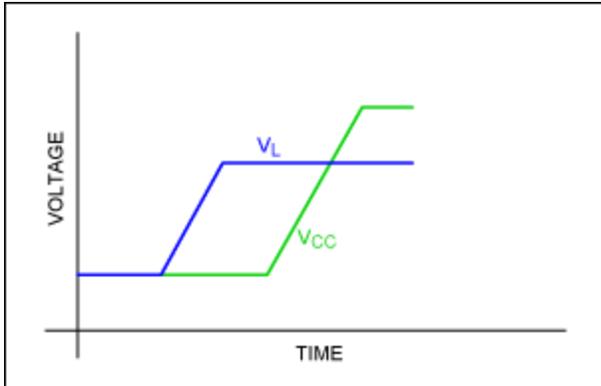


Figure 1. V_L rises in advance of the V_{CC} rising, resulting in a good power-up.

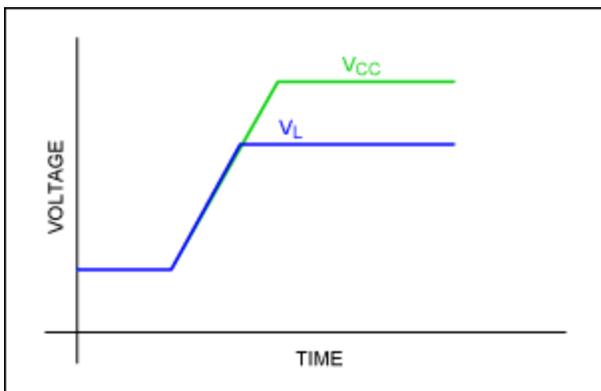


Figure 2. V_L rises coincidentally with the V_{CC} rising, resulting in a good power-up.

Case 2: When V_L Rises After V_{CC}

In the situation where V_L starts rising after V_{CC} begins to rise at power-up, some care must be taken (**Figure 3**). For proper power-up, users must ensure that V_{CC} has settled before V_L starts rising.

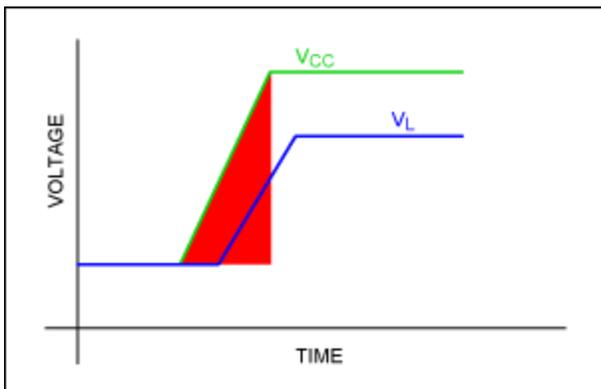


Figure 3. V_L rises too soon after V_{CC} , resulting in a bad power-up.

V_L needs to start rising after V_{CC} has settled (outside of the red triangle illustrated in **Figure 4**).

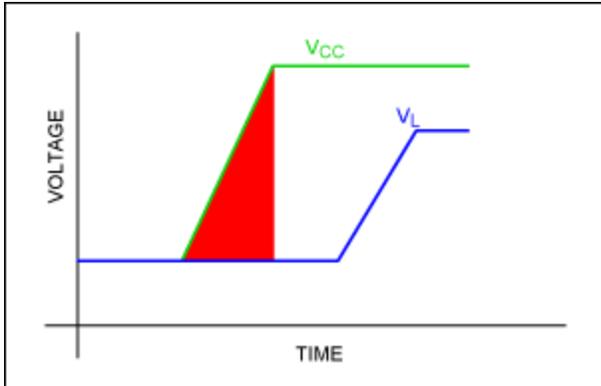


Figure 4. V_L rises after V_{CC} has settled, resulting in a good power-up.

To provide a safety margin against variations in production and sequencing external power-supply circuits, it is recommended that the delay from V_{CC} rising to V_L rising be at least twice the rise time of the V_{CC} supply.

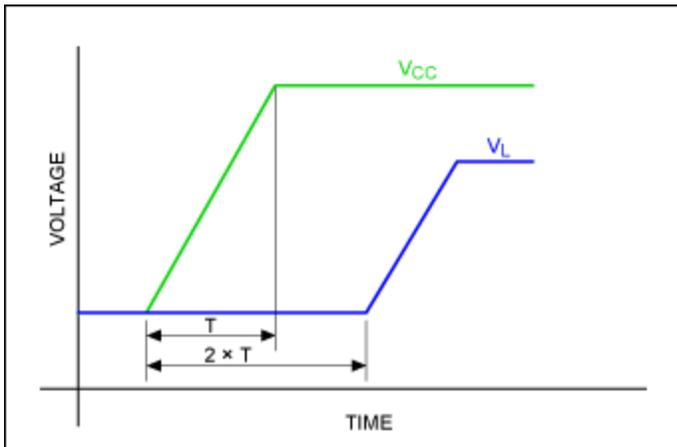


Figure 5. Definition and requirements for safe timing with margin.

Detailed Analysis of Power Sequencing

Often, power supply rails rise as shown in the previous figures. In some cases, however, the point where a power-supply transition ends is not so clear. This section describes a quantitative means to analyze a given specific scenario where V_L rises after V_{CC} . This method ensures that there is sufficient delay for correct power-up sequencing.

To determine this, four time measurements must be taken. Two of these measurements are with respect to specific voltage levels on V_{CC} , and the other two are with respect to specific voltage levels on V_L . All four measurements are to be taken from a single scope capture.

The following time measurements need to be taken:

1. $T_{V_{CC}90}$ = the time at which the V_{CC} rising waveform has reached 90% of its final value, which should be 90% of 5V.
2. $T_{V_{CC}10}$ = the time at which the V_{CC} rising waveform has reached 10% of its final value, which

should be 10% of 5V.

3. T_{VL90} = the time at which the V_L rising waveform has reached 90% of its final value, which will be 90% of 3.3V or 90% of 2.5V.
4. T_{VL10} = the time at which the V_L rising waveform has reached 10% of its final value, which will be 10% of 3.3V or 10% of 2.5V.

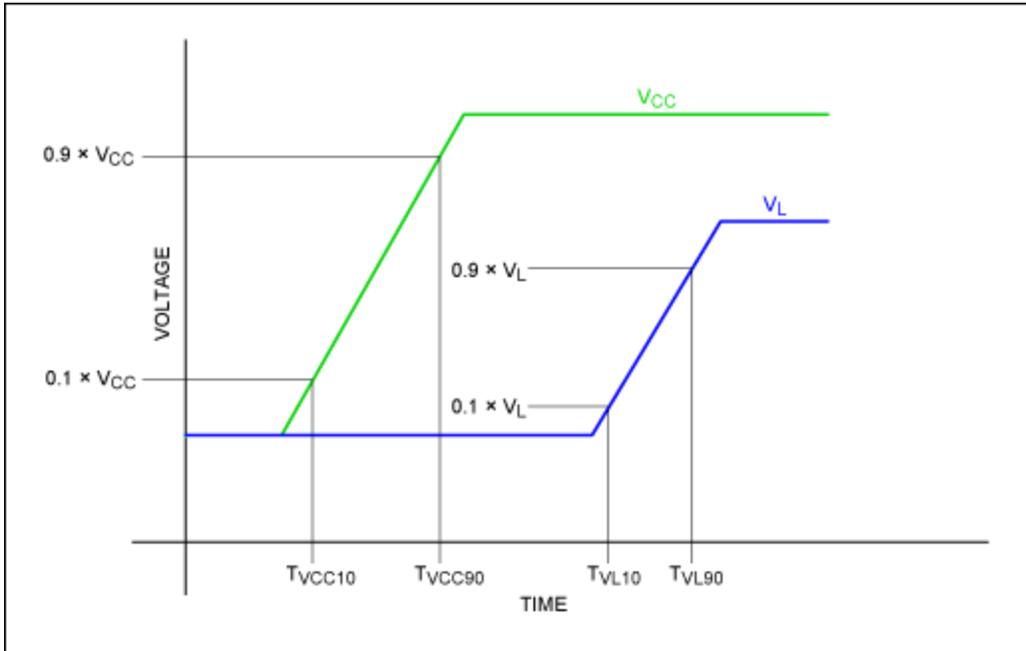


Figure 6. The time measurements needed to analyze a scenario where V_L rises after V_{CC} .

Now, perform the following calculations:

$$T1 = 2.5(T_{VCC90} - T_{VCC10})$$

$$T2 = \frac{T_{VCC90} - T_{VCC10}}{8}$$

$$T3 = \frac{T_{VL90} - T_{VL10}}{8}$$

To ensure sufficient margin between V_{CC} and V_L rising at power-up, the external power supply design must guarantee that:

$$T_{VL10} \geq T_{VCC10} + T1 - T2 + T3$$

Conclusion

This application note has described the correct power-up conditions for the MAX14885E VGA dual-graphics crossover switch. It has recommended how much margin to use in the sequencing delay if V_L succeeds V_{CC} when powering up. It has also provided a set of calculations to use when the trailing edge of the power supply ramp is not clearly defined.

Related Parts

MAX14885E	Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch	Free Samples
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