# **Bipolar Power Transistors**

## **PNP Silicon**

# **NJT4030P, NJV4030P**

### **Features**

- Epoxy Meets UL 94, V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	40	Vdc
Collector-Base Voltage	V <sub>CB</sub>	40	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	6.0	Vdc
Base Current - Continuous	I <sub>B</sub>	1.0	Adc
Collector Current - Continuous	I <sub>C</sub>	3.0	Adc
Collector Current - Peak	I <sub>CM</sub>	5.0	Adc
ESD - Human Body Model	НВМ	3B	V
ESD - Machine Model	MM	С	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
	P <sub>D</sub>	2.0 0.80	W
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$egin{array}{c} R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	11 64 155	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

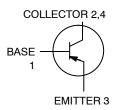
- 1. Mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material.
- 2. Mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material.

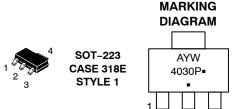


### ON Semiconductor®

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# PNP TRANSISTOR 3.0 AMPERES 40 VOLTS, 2.0 WATTS





A = Assembly Location

' Year

W = Work Week

4030P = Specific Device Code ■ Pb–Free Package

(Note: Microdot may be in either location)

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NJT4030PT1G	SOT-223	1000 / Tape &
NJV4030PT1G	(Pb-Free)	Reel
NJT4030PT3G	SOT-223	4000 / Tape &
NJV4030PT3G	(Pb-Free)	Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NJT4030P, NJV4030P

# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 10 mAdc, I <sub>B</sub> = 0 Adc)	V <sub>CEO(sus)</sub>	40	_	-	Vdc
Emitter-Base Voltage (I <sub>E</sub> = 50 µAdc, I <sub>C</sub> = 0 Adc)	V <sub>EBO</sub>	6.0	-	-	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 40 Vdc)	I <sub>CBO</sub>	-	_	100	nAdc
Emitter Cutoff Current (V <sub>BE</sub> = 6.0 Vdc)	I <sub>EBO</sub>	-	-	100	nAdc
ON CHARACTERISTICS (Note 3)	·				
Collector–Emitter Saturation Voltage ( $I_C = 0.5 \text{ Adc}$ , $I_B = 5.0 \text{ mAdc}$ ) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 10 \text{ mAdc}$ ) ( $I_C = 3.0 \text{ Adc}$ , $I_B = 0.3 \text{ Adc}$ )	V <sub>CE(sat)</sub>	- - -	- - -	0.150 0.200 0.500	Vdc
Base–Emitter Saturation Voltage ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	V <sub>BE(sat)</sub>	-	-	1.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 2.0 Vdc)	V <sub>BE(on)</sub>	-	-	1.0	Vdc
DC Current Gain $(I_C = 0.5 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc})$ $(I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc})$ $(I_C = 3.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc})$	h <sub>FE</sub>	220 200 100	- - -	- 400 -	-
DYNAMIC CHARACTERISTICS					
Output Capacitance (V <sub>CB</sub> = 10 Vdc, f = 1.0 MHz)	C <sub>ob</sub>	-	40	-	pF
Input Capacitance (V <sub>EB</sub> = 5.0 Vdc, f = 1.0 MHz)	C <sub>ib</sub>	-	130	-	pF
Current–Gain – Bandwidth Product (Note 4) (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 10 V, F <sub>test</sub> = 1.0 MHz)	f <sub>T</sub>	-	160	-	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

<sup>4.</sup>  $f_T = |h_{FE}| \bullet f_{test}$ 

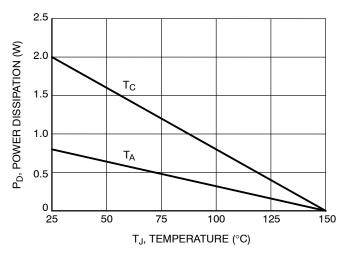


Figure 1. Power Derating

<sup>3.</sup> Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

## **NJT4030P, NJV4030P**

### **TYPICAL CHARACTERISTICS**

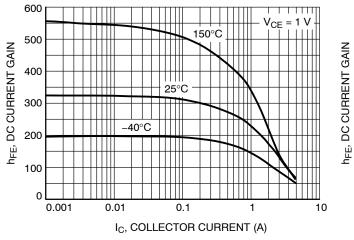


Figure 2. DC Current Gain

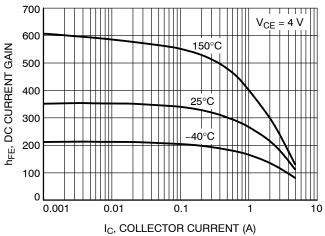


Figure 3. DC Current Gain

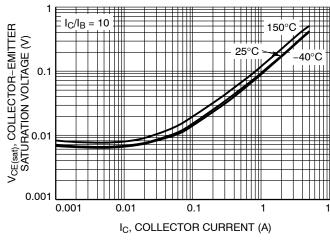


Figure 4. Collector-Emitter Saturation Voltage

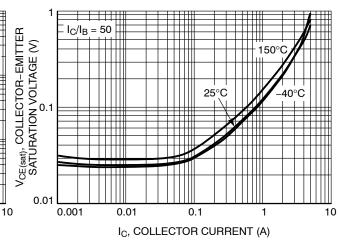


Figure 5. Collector-Emitter Saturation Voltage

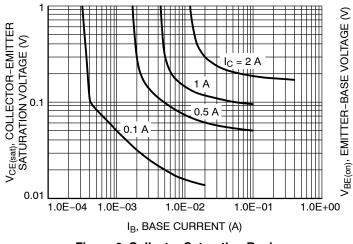


Figure 6. Collector Saturation Region

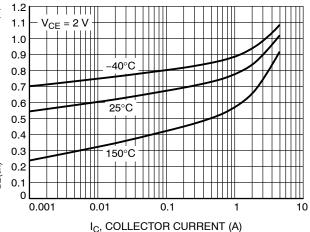


Figure 7. V<sub>BE(on)</sub> Voltage

## **NJT4030P, NJV4030P**

### TYPICAL CHARACTERISTICS

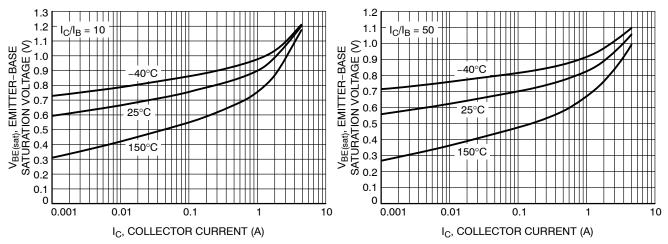


Figure 8. Base-Emitter Saturation Voltage

Figure 9. Base-Emitter Saturation Voltage

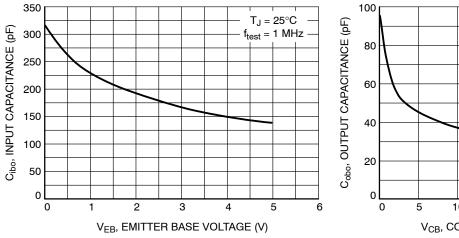


Figure 10. Input Capacitance

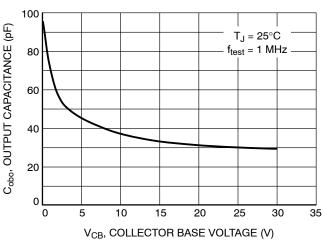


Figure 11. Output Capacitance

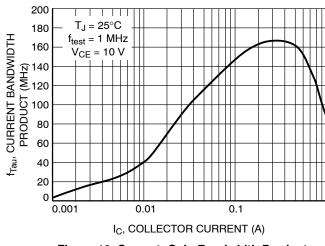


Figure 12. Current-Gain Bandwidth Product

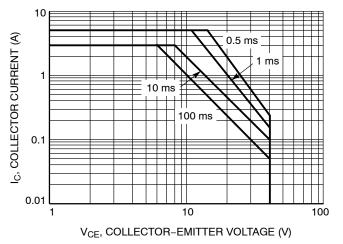
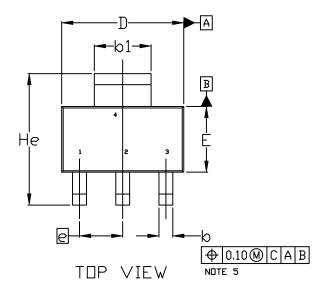


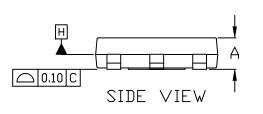
Figure 13. Safe Operating Area

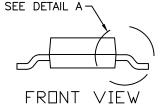


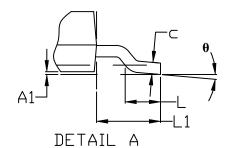
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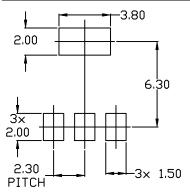




#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5. ALLIS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS 6 AND 61.

	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	1.50	1.63	1.75	
A1	0.02	0.06	0.10	
b	0.60	0.75	0.89	
b1	2.90	3.06	3.20	
c	0.24	0.29	0.35	
D	6.30	6.50	6.70	
E	3.30	3.50	3.70	
е	2.30 BSC			
L	0.20			
L1	1.50	1.75	2.00	
He	6.70	7.00	7.30	
θ	0°		10°	



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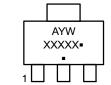
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STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

# GENERIC MARKING DIAGRAM\*



A = Assembly Location

Y = Year W = Work Week

 $XXXXX \ = Specific \ Device \ Code$ 

= Pb-Free Package

(Note: Microdot may be in either location)
\*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may
not follow the Generic Marking.

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