Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

Semiconductor

FEDL9473-01
Issue Date: Aug. 21, 2008

ML9473

1/3, 1/4, 1/5 Duty 60 Output LCD Driver

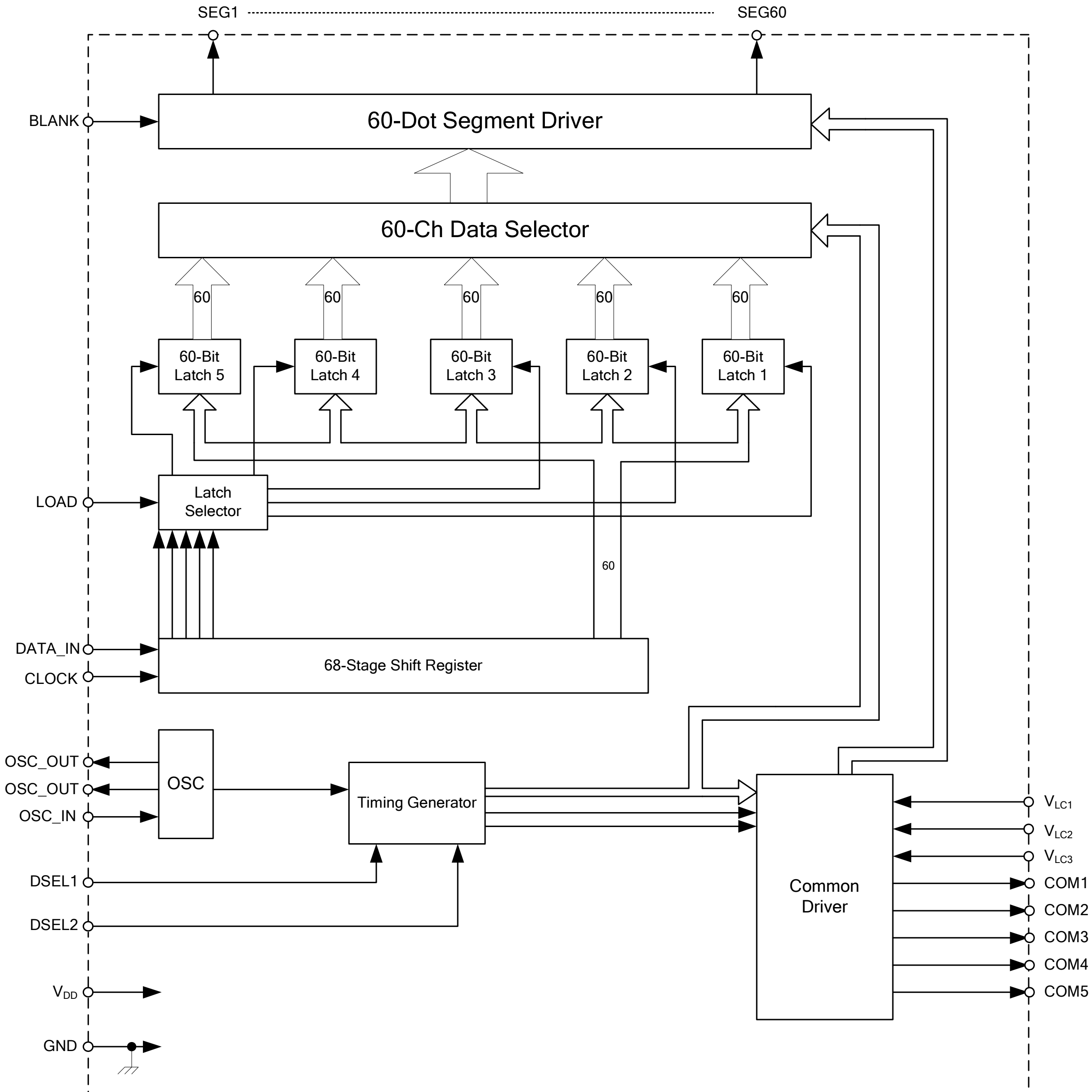
GENERAL DESCRIPTION

The ML9473 is a LCD driver for dynamic display providing 3-duty-switchable pins (1/3, 1/4, 1/5 duty). It can directly drive LCDs of up to 300, 240 and 180 segments when 1/5, 1/4 and 1/3 duty are selected respectively.

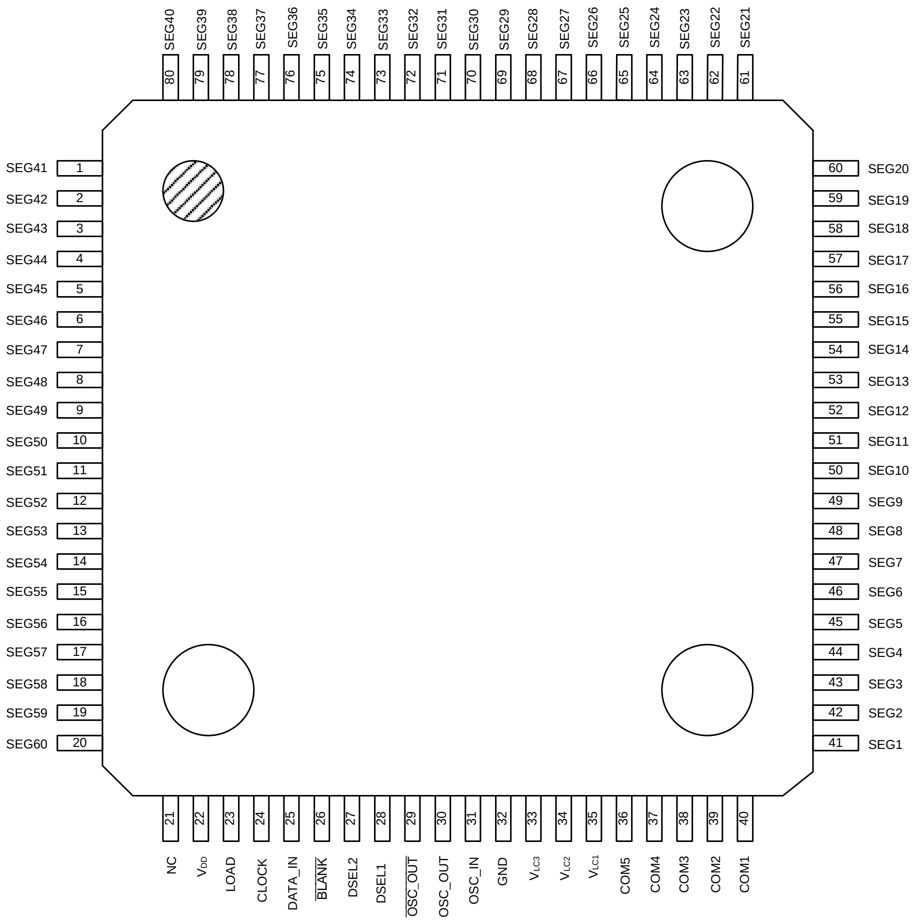
FEATURES

- Operating range
  Supply voltage : 3.0 to 5.5 V
  Operating temperature range : –40 to + 105°C
- Segment output : 60 pins
  1/5 duty : Up to 300 segments can be displayed.
  1/4 duty : Up to 240 segments can be displayed.
  1/3 duty : Up to 180 segments can be displayed.
- Serial transfer clock frequency : 4 MHz
- Serical interface with CPU :Through three input pins (DATA_IN, LOAD, and CLOCK)
- Built-in oscillator circuit for COMMON signals
- One-to-one correspondence between input data and output data
  When input data is at "H" level : Display goes on.
  When input data is at "L" level : Display goes off.
- The entire display can be turned off. ($\overline{\text{BLANK}}$ pin)
- Package options
  80-pin plastic TQFP (TQFP80-P-1212-0.50-K) (Product name: ML9473TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic TQFP

PIN DESCRIPTION

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>OSC_IN
OSC_OUT
$\overline{\mathrm{OSC\_OUT}}$</td><td>I
O
O</td><td>Pins for oscillation. The oscillator circuit is configured by externally connecting two resistors and a capacitor. Make the wiring length as short as possible, because the resistor connected to the OSC_IN pin has a higher value and the circuit is susceptible to external noise.</td></tr>
<tr><td>DATA_IN</td><td>I</td><td>Serial data input pin. The display goes on when input data is at a “H” level, and it goes off when input data is at a “L” level.</td></tr>
<tr><td>CLOCK</td><td>I</td><td>Shift clock input pin. Data from the DATA_IN pin is transferred in synchronization with the rising edge of the shift clock.</td></tr>
<tr><td>LOAD</td><td>I</td><td>Load signal input pin. Serially input data is transferred to the 60-bit latch at “H” level of this load signal, then held at “L” level.</td></tr>
<tr><td>$\overline{\mathrm{BLANK}}$</td><td>I</td><td>Input pin that turns off all segments. The entire display goes off when “L” level is applied to this pin. The display returns to the previous state when “H” level is applied.</td></tr>
<tr><td>DSEL1
DSEL2</td><td>I
I</td><td>Input pins to select 1/3, 1/4, or 1/5 duty. Following shows how each duty is selected.
<table>
<tr><th>DSEL2</th><th>DSEL1</th><th>Duty selected</th></tr>
<tr><td>L</td><td>L</td><td>1/3</td></tr>
<tr><td>L</td><td>H</td><td>1/4</td></tr>
<tr><td>H</td><td>X</td><td>1/5</td></tr>
</table>
X: Don’t care</td></tr>
<tr><td>COM1 to
COM5</td><td>O</td><td>Display output pins for LCD. These pins are connected to the COMMON side of the LCD panel.</td></tr>
<tr><td>SEG1 to
SEG60</td><td>O</td><td>Display output pins for LCD. Theses pins are connected to the SEGMENT side of the LCD panel. For the correspondence between the output of these pins and input data, see the “Data Structure” Section.</td></tr>
<tr><td>V_{LC1}, V_{LC2},
V_{LC3}</td><td>—</td><td>Bias pins for LCD driver. Through these pins, bias voltages for the LCD are externally supplied. The bias potential must meet the following condition:
$V_{DD} > V_{LC1} \geq V_{LC2} > V_{LC3}$ =GND</td></tr>
<tr><td>V_{DD}, GND</td><td>—</td><td>Supply voltage pin and ground pin.</td></tr>
</table>

Note: Built-in schmitt circuit is used for all input pins.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to 6.5	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to 150	°C
Power Dissipation	P_D	Ta < 105°C	650	mW
Output Current	I_O	—	–2.0 to 2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	V_{LC3} = GND	3.0 to 5.5	V
CLOCK Frequency	f_{CP}	—	0.75 to 4	MHz
Operating Temperature	Ta	—	–40 to 105	°C

Oscillator Circuit

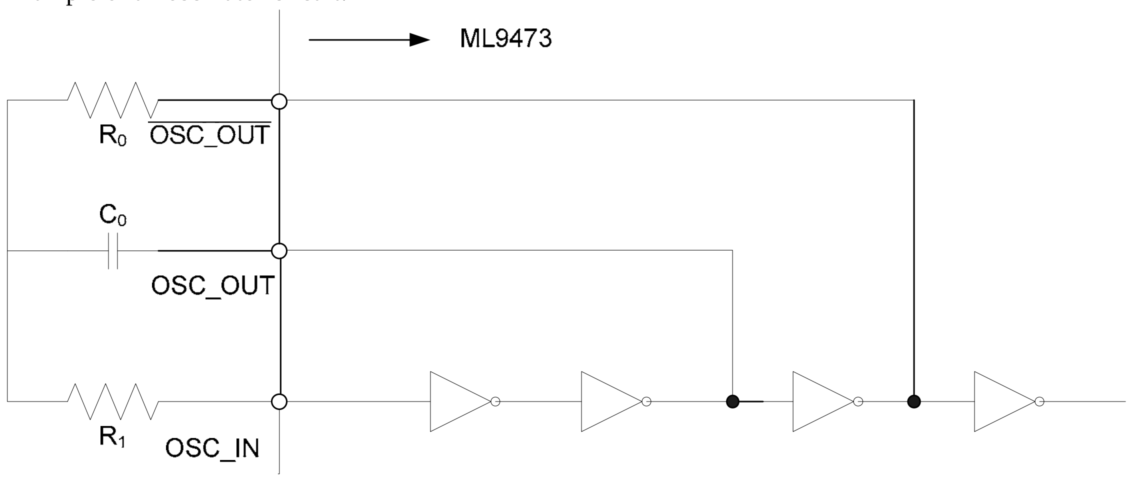
Parameter	Symbol	Applicable pin	Condition	Min.	Max.	Unit
Oscillator Resistance	R_0	$\overline{\text{OSC\_OUT}}$	—	20	120	kΩ
Oscillator Capacitance	C_0	OSC_OUT	—	0.00047	0.01	μF
Current Limiting Resistance	R_1	OSC_IN	—	62	360	kΩ
Common Signal Frequency	f_{COM}	COM1 to COM5	—	25	250	Hz

Note: See Section, “Reference Data”, for the resistor and capacitor values in the table.

RC Values in Oscillator Circuit

Parameter	Symbol	Applicable pin	1/3 duty	1/4 duty	1/5 duty	Unit
Oscillator Resistance	R_0	$\overline{\text{OSC\_OUT}}$	68	51	43	kΩ
Oscillator Capacitance	C_0	OSC_OUT	0.001	0.001	0.001	μF
Current Limiting Resistance	R_1	OSC_IN	220	160	130	kΩ

Example of an oscillator circuit:



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 3.0 to 5.5 V, Ta = –40 to +105°C, unless otherwise specified)

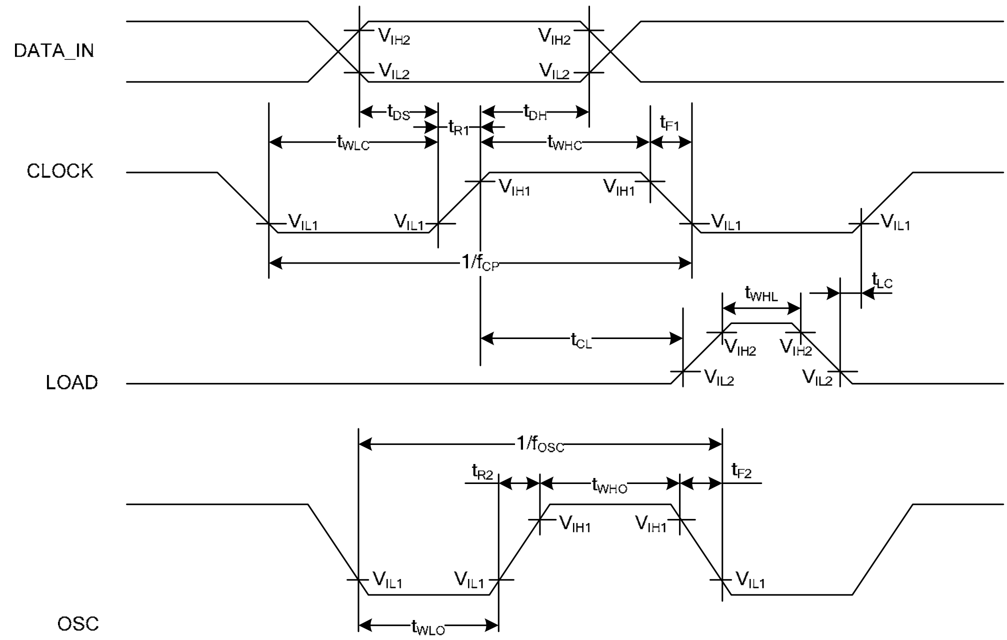
Parameter	Symbol	Applicable pin	Condition		Min.	Max.	Unit
"H" Input Voltage 1	V_{IH1}	CLOCK, OSC_IN	—		0.85 V_{DD}	V_{DD}	V
"L" Input Voltage 1	V_{IL1}	CLOCK, OSC_IN	—		GND	0.15 V_{DD}	V
"H" Input Voltage 2	V_{IH2}	*1	—		0.8 V_{DD}	V_{DD}	V
"L" Input Voltage 2	V_{IL2}	*1	—		GND	0.2 V_{DD}	V
"H" Input Current	I_{IH}	All input pins	V_{DD} = 5.5 V, V_I = V_{DD}		—	10	μA
"L" Input Current	I_{IL}	All input pins	V_{DD} = 5.5 V, V_I = 0 V		–10	—	μA
COMMON Output Voltage	V_{OC0a}	COM1 - COM5	V_{DD} = 3.0 V	I_O = –100 μA	V_{DD} –1	—	V
	V_{OC1}			I_O = ±100 μA *3	V_{LC1} –1	V_{LC1} +1	V
	V_{OC2}			I_O = ±100 μA *4	V_{LC2} –1	V_{LC2} +1	V
	V_{OC3}			I_O = +100 μA *5	—	V_{LC3} +1	V
Segment Output Voltage	V_{OS0}	SEG_1 - SEG_{60},	V_{DD} = 3.0 V	I_O = –10 μA	V_{DD} –1	—	V
	V_{OS1}			I_O = ±10 μA *3	V_{LC1} –1	V_{LC1} +1	V
	V_{OS2}			I_O = ±10 μA *4	V_{LC2} –1	V_{LC2} +1	V
	V_{OS3}			I_O = +10 μA *5	—	V_{LC3} +1	V
Supply Current	I_{DD}	V_{DD}	V_{DD} = 5.0 V, no load. *2		—	0.5	mA

*1 Applies to all input pins excluding CLOCK and OSC_IN.
*2 R_0 = 51 kΩ R_1 = 160 kΩ C_0 = 0.001 μF
*3 V_{LC1} = 2.0V
*4 V_{LC2} = 1.0V
*5 V_{LC3} = 0V

AC Characteristics

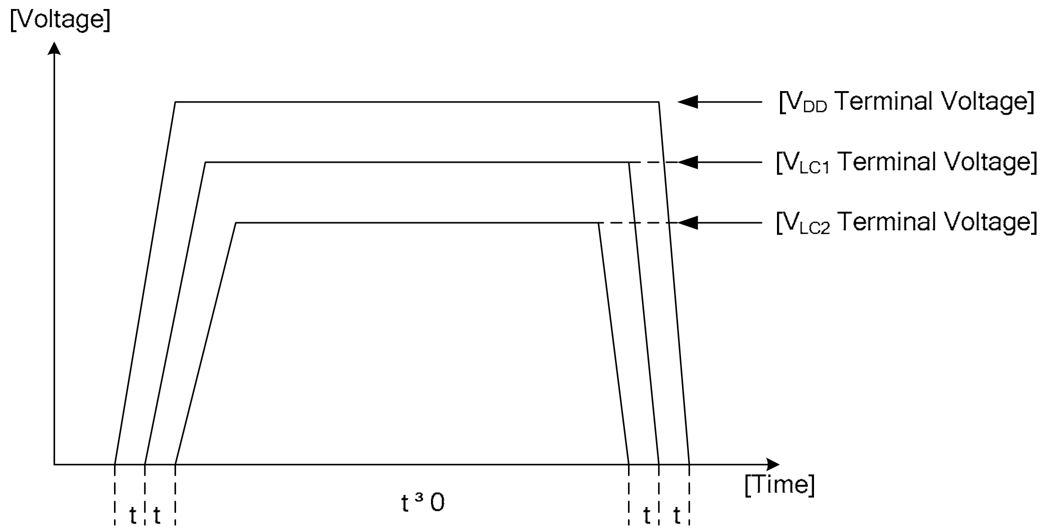
(V_{DD} =3.0 to 5.5V, Ta = –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock “H” Time	t_{WHC}	—	70	—	—	ns
Clock “L” Time	t_{WLC}	—	70	—	—	ns
Data Set-up Time	t_{DS}	—	50	—	—	ns
Data Hold Time	t_{DH}	—	50	—	—	ns
Load “H” Time	t_{WHL}	—	100	—	—	ns
Clock-to-load Time	t_{CL}	—	100	—	—	ns
Load-to-Clock Time	t_{LC}	—	100	—	—	ns
Clock Rise time, Fall time	t_{R1}, t_{F1}	—	—	—	50	ns
OSC_IN Input Frequency	f_{OSC}	—	—	—	20	kHz
OSC_IN “H” Time	t_{WHO}	—	20	—	—	μs
OSC_IN “L” Time	t_{WLO}	—	20	—	—	μs
OSC_IN Rise time, Fall time	t_{R2}, t_{F2}	—	—	—	100	ns



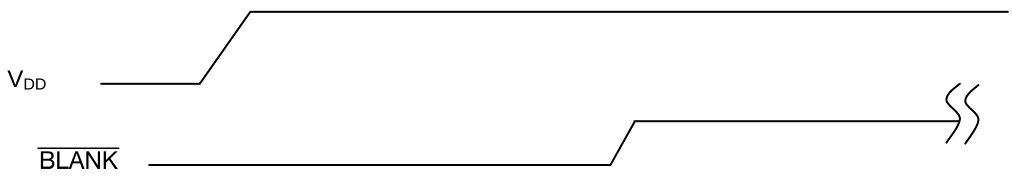
(V_{IH1} = 0.85V_{DD} V_{IL1} = 0.15V_{DD})
(V_{IH2} = 0.8V_{DD} V_{IL2} = 0.2V_{DD})

POWER-ON/OFF TIMING



* V_{LC1}, V_{LC2} are applied when V_{DD} is applied to external bias resistor.

INITIAL SIGNAL TIMING

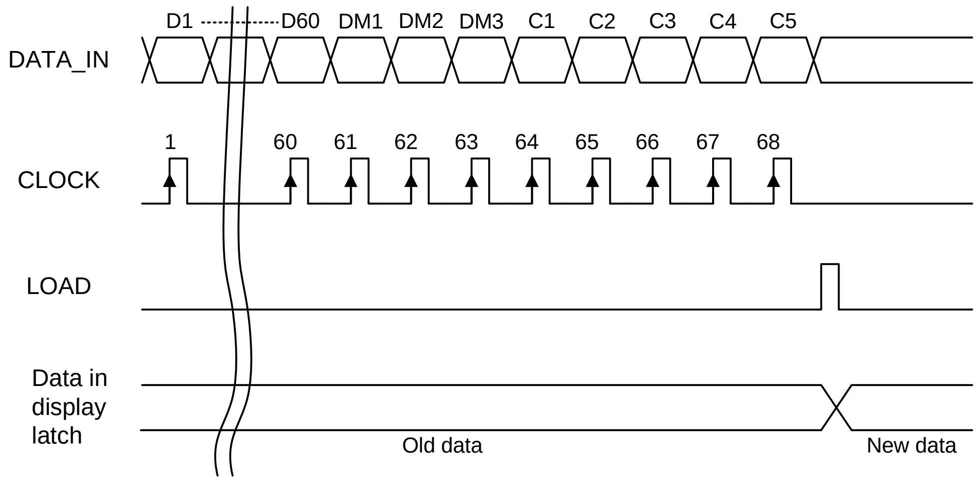


* Once V_{DD} is applied, $\overline{\text{BLANK}}$ should be applied to ‘L’ level to make all SEGMENTs off until first group of display data is latched.

FUNCTIONAL DESCRIPTION

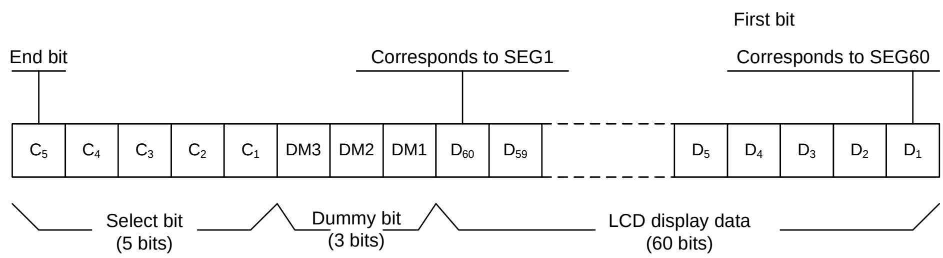
Operation

As shown in "Data Structure", the display data consists of the data field corresponding to the output for turning the segments on or off and the select field that selects field that selects the input block of data. Data input to the DATA_IN pin is loaded into the 68-bit shift register, transferred to the 60-bit latch while the load signal is at "H" level, and then output via the 60-dot segment driver.



Data Structure

Input data



Correspondence between select bits and COM1 to COM5

C5	C4	C3	C2	C1	Description
0	0	0	0	1	Display data corresponding to COM1
0	0	0	1	0	Display data corresponding to COM2
0	0	1	0	0	Display data corresponding to COM3
0	1	0	0	0	Display data corresponding to COM4
1	0	0	0	0	Display data corresponding to COM5

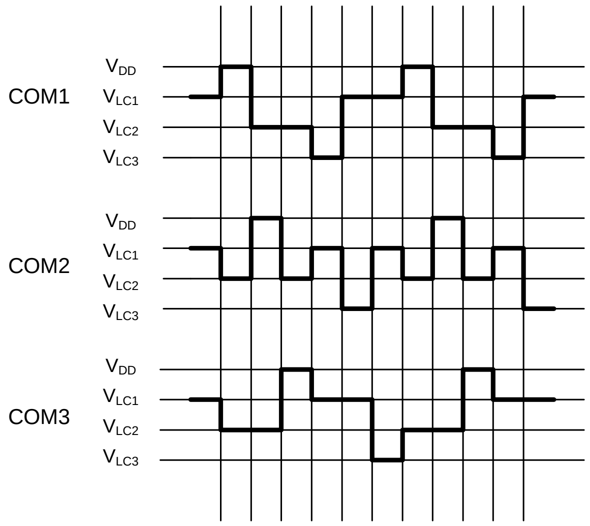
Notes: 1. Arbitrary data can be set for the dummy bits.

2. Select bit, C_1 to C_5, selects 60-bit latches that correspond to COM1 to COM5, respectively. Therefore, if "1" is set for more than one select bit, data is set to all the corresponding 60-bit latches.

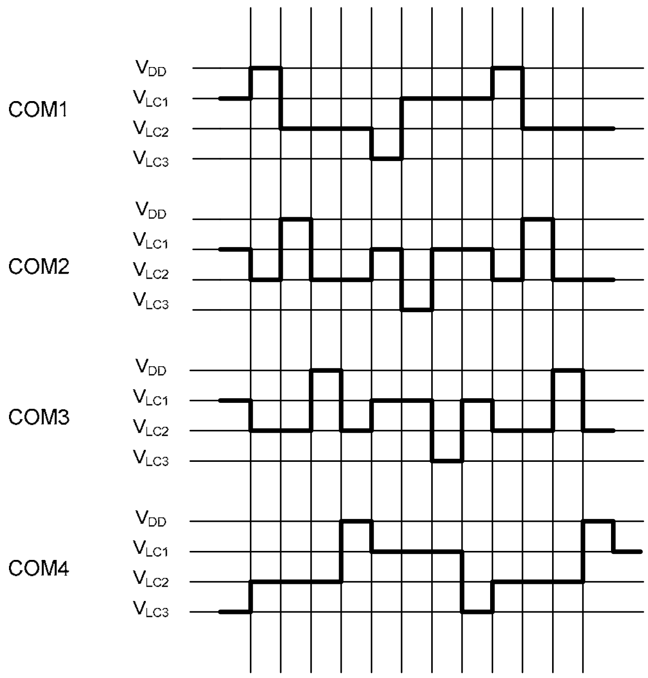
Example:

If "1" is set to all the select bits C_1 to C_5, the display data of D_1 to D_{60} is set to all the 60-bit latches that correspond to COM1 to COM5.

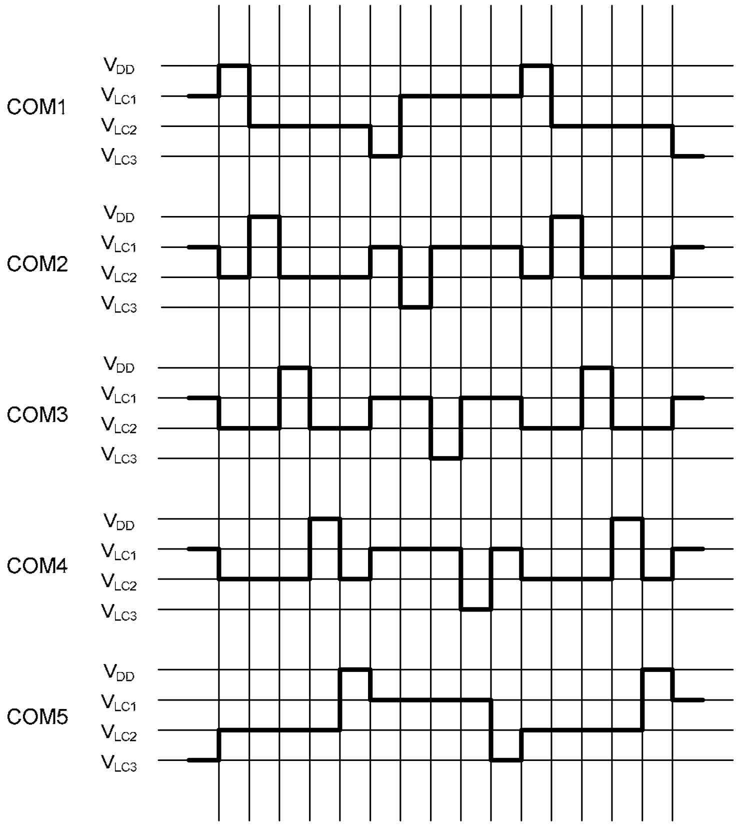
COM1 – COM5 Timing Chart:



1/3 DUTY COM
TIMING



1/4 DUTY COM
TIMING



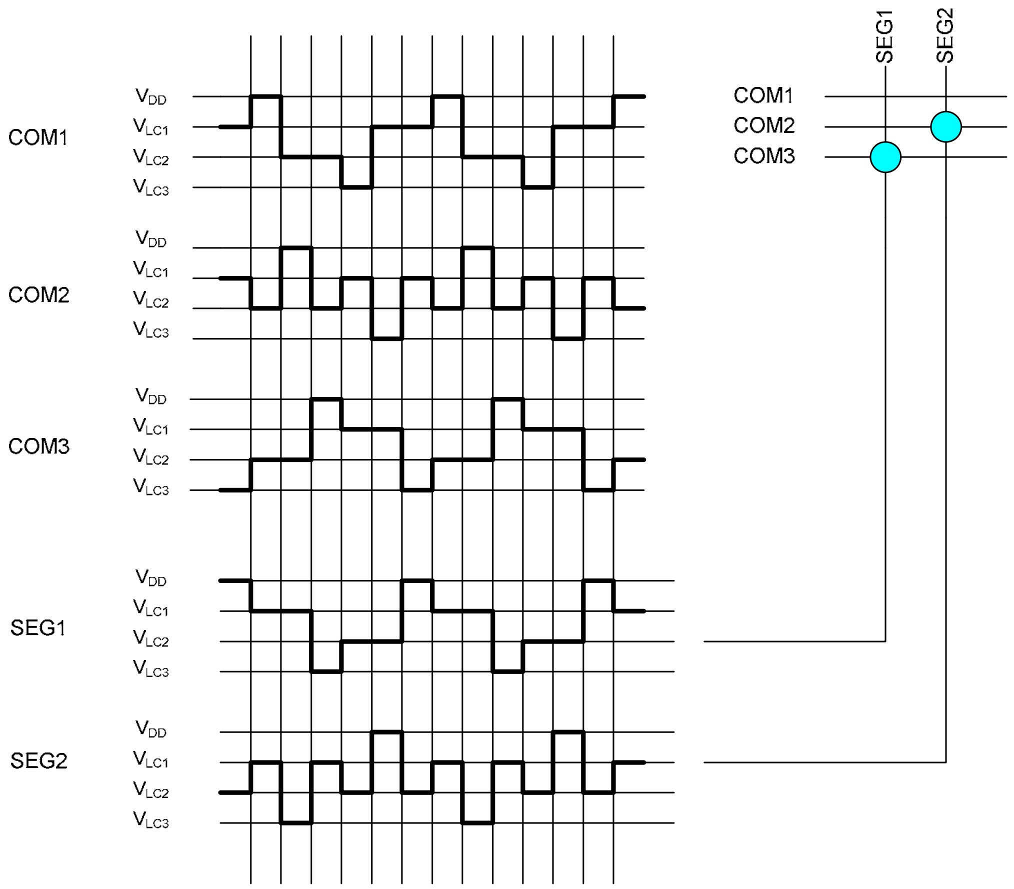
1/5 DUTY COM
TIMING

SEGn True Value Table:

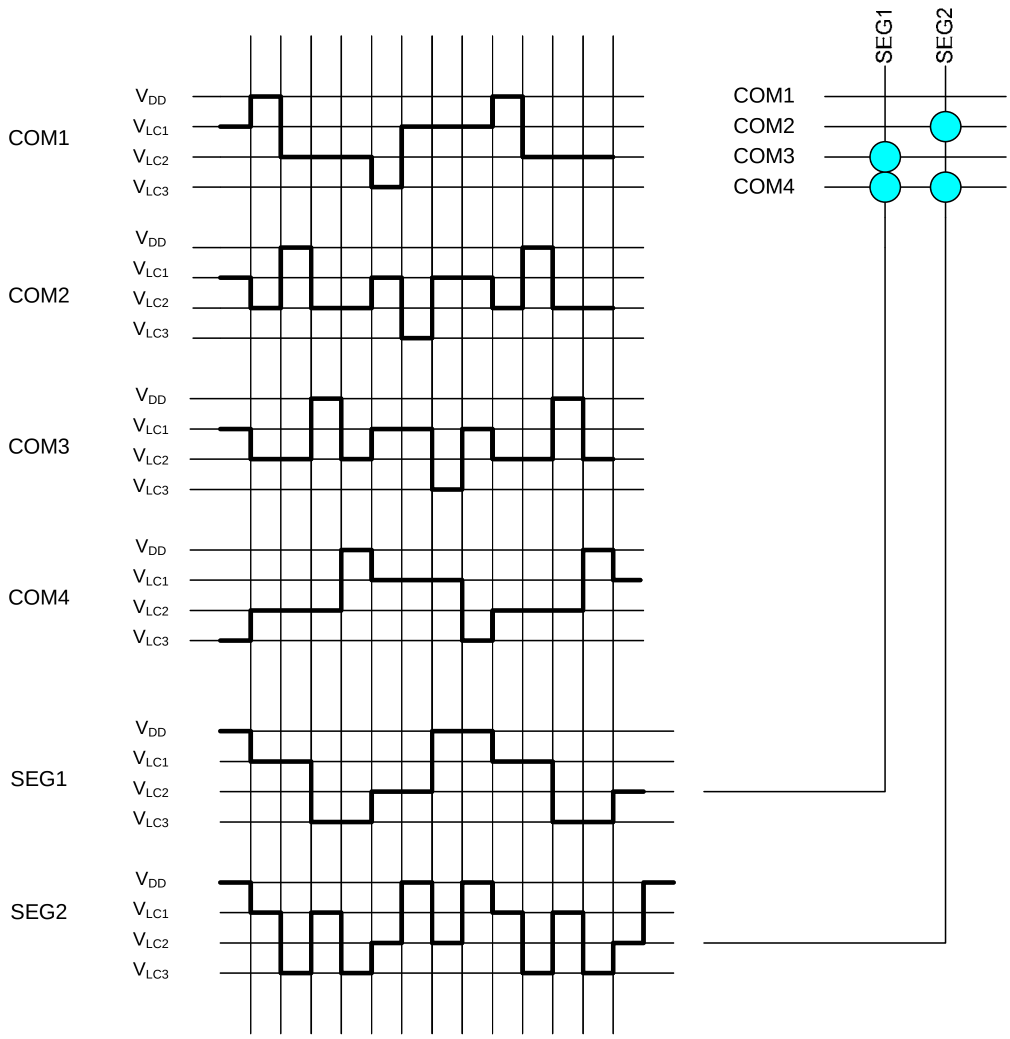
LATCH1	LATCH2	LATCH3	LATCH4	LATCH5	COM1	COM2	COM3	COM4	COM5	SEGn
0	0	0	0	1	“H”	“M2”	“M2”	“M2”	“M2”	“M1”
					“L”	“M1”	“M1”	“M1”	“M1”	“M2”
					“M2”	“H”	“M2”	“M2”	“M2”	“M1”
					“M1”	“L”	“M1”	“M1”	“M1”	“M2”
					“M2”	“M2”	“H”	“M2”	“M2”	“M1”
					“M1”	“M1”	“L”	“M1”	“M1”	“M2”
					“M2”	“M2”	“M2”	“H”	“M2”	“M1”
					“M1”	“M1”	“M1”	“L”	“M1”	“M2”
					“M2”	“M2”	“M2”	“M2”	“H”	“L”
					“M1”	“M1”	“M1”	“M1”	“L”	“H”

*Note: “H” = V_{DD}; “M1” = V_{LC1}; “M2” = V_{LC2}; “L” = V_{LC3}=GND

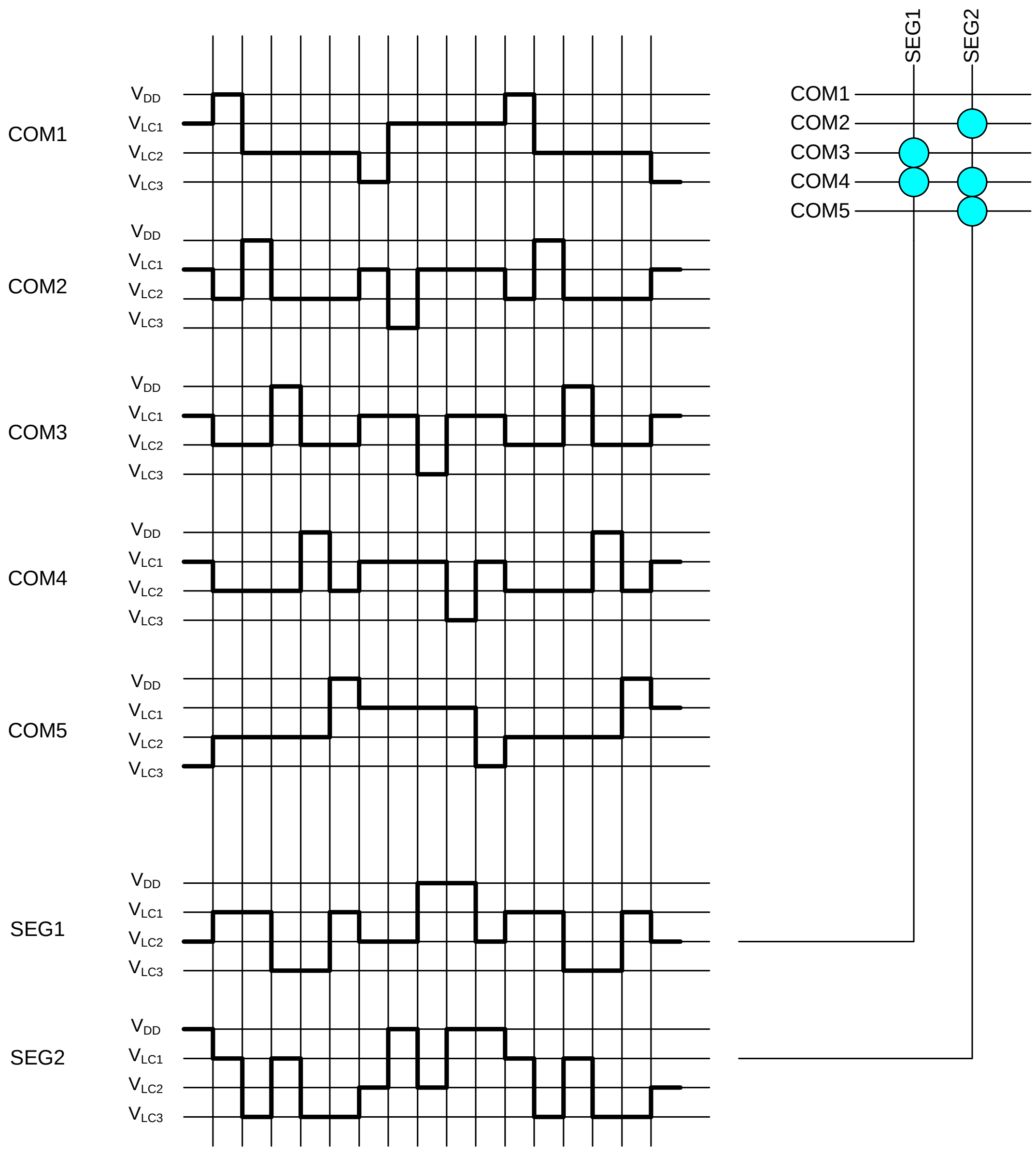
Timing Chart FOR 1/3 DUTY DRIVE MODE:



Timing Chart FOR 1/4 DUTY DRIVE MODE:

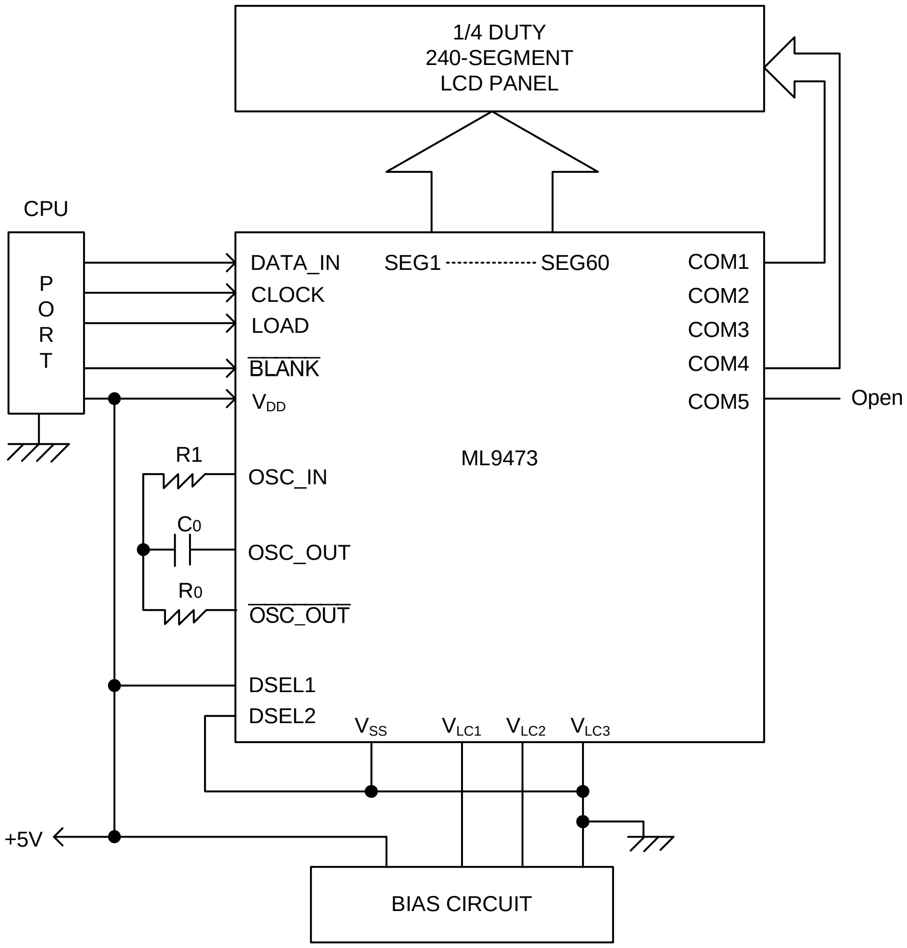


Timing Chart FOR 1/5 DUTY DRIVE MODE:



APPLICATION CIRCUITS

(For 1/4 duty)



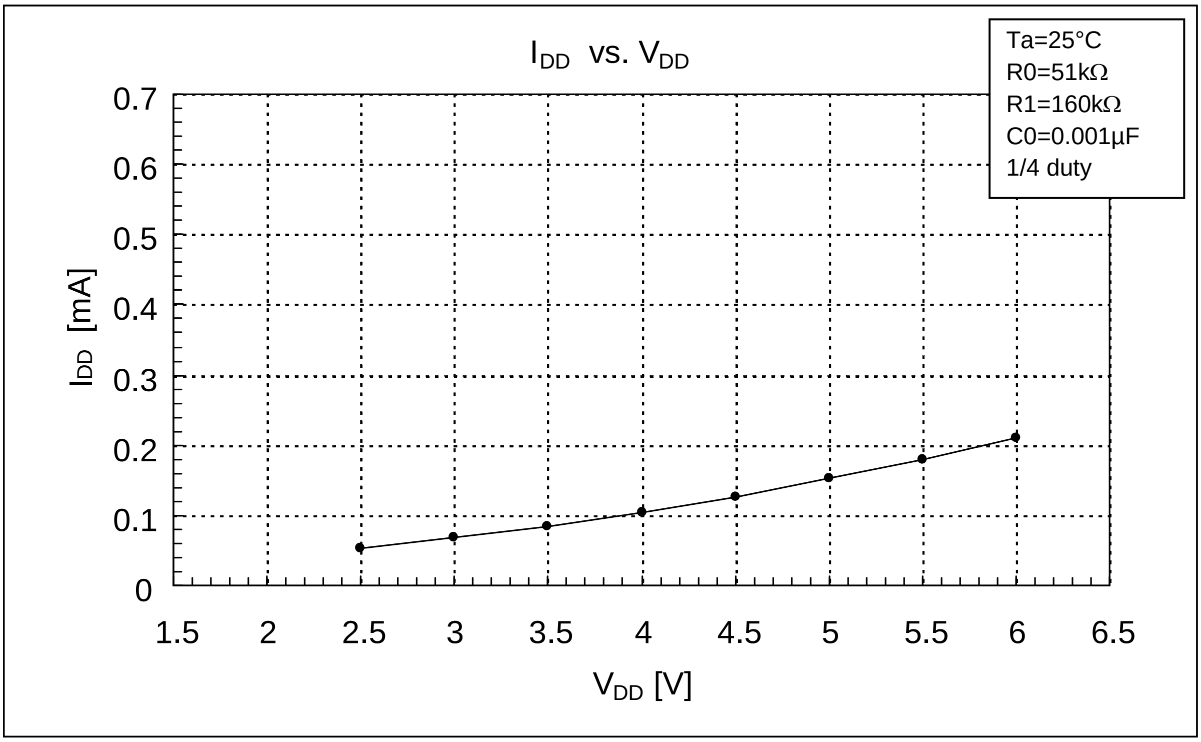
REFERENCE DATA

The data shown in this section is for reference (a metal film resistor and a film capacitor are used). Resistor and capacitor values must be determined based on experiments.
Use the following expression to convert oscillation frequency to COMMON frame frequency (or vice versa):

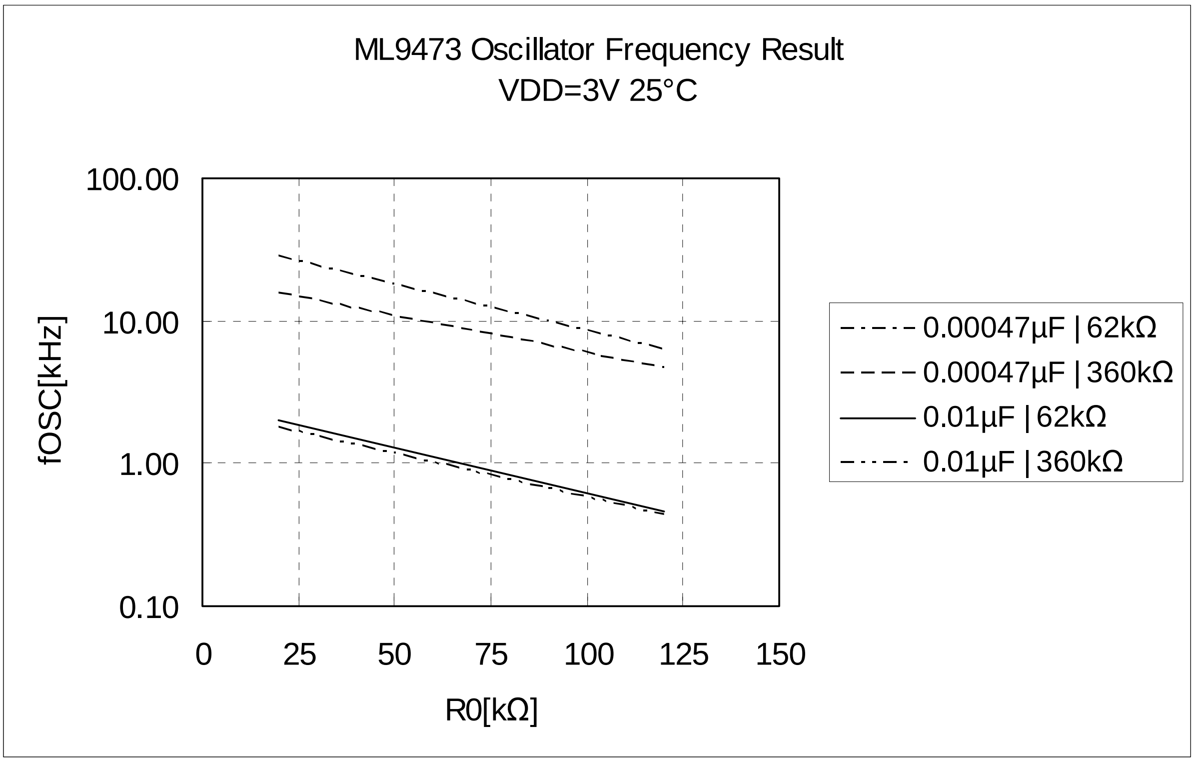
$$f_{COM}=f_{OSC} \times Duty/16$$

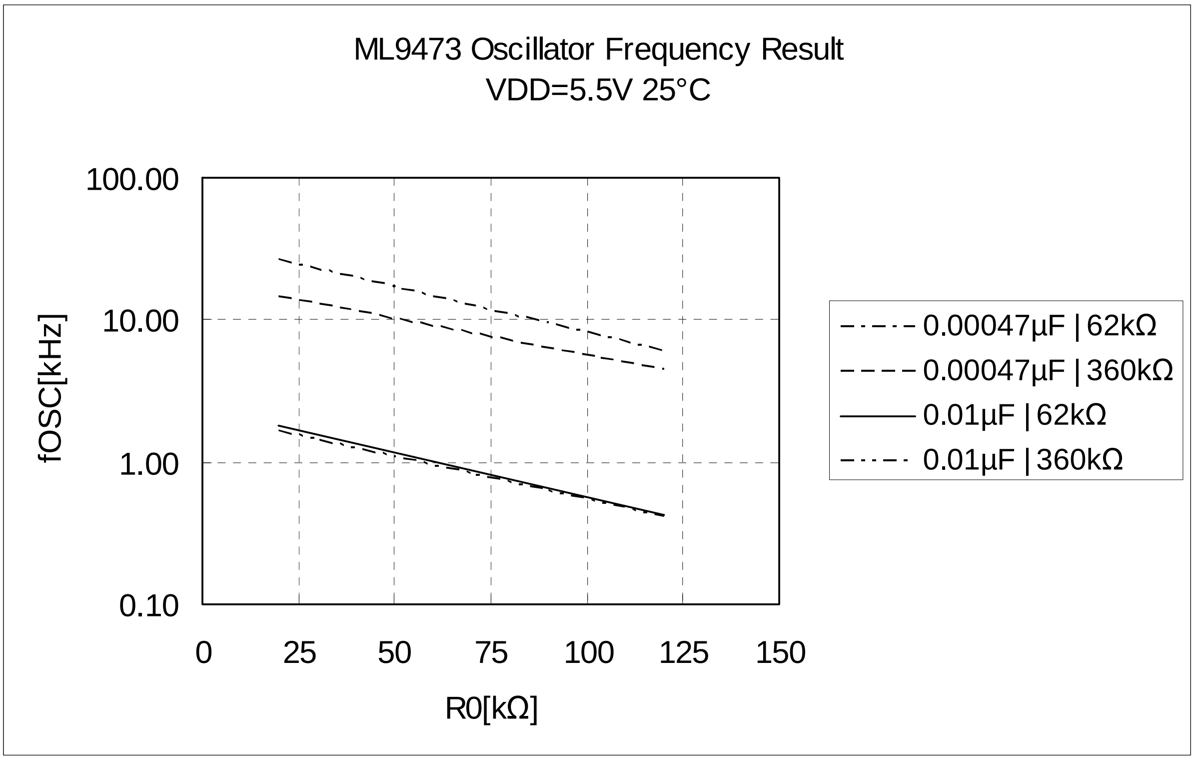
f_{COM} : COMMON frame frequency
f_{OSC} : Oscillation frequency
Duty : e.g., 1/4 for 1/4 duty

For example, if f_{COM}=100Hz at 1/5 duty, the oscillation frequency is f_{OSC} =8000Hz.



fOSC---R0,C0

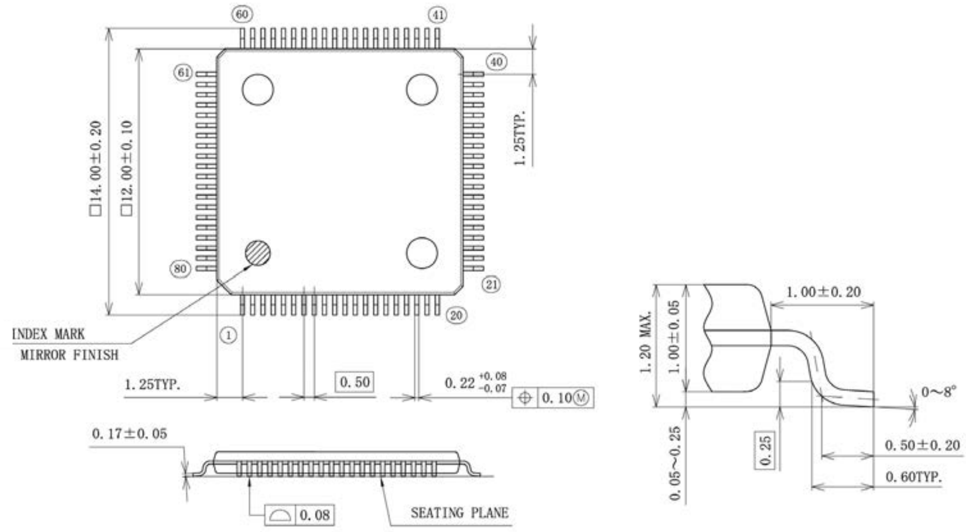

ML9473 Oscillator Frequency Result
VDD=3V 25°C
100.00
10.00
1.00
0.10
fOSC[kHz]
0
25
50
75
100
125
150
R0[kΩ]
0.00047μF | 62kΩ
0.00047μF | 360kΩ
0.01μF | 62kΩ
0.01μF | 360kΩ


ML9473 Oscillator Frequency Result
VDD=5.5V 25°C
100.00
10.00
1.00
0.10
fOSC[kHz]
0
25
50
75
100
125
150
R0[kΩ]
0.00047μF | 62kΩ
0.00047μF | 360kΩ
0.01μF | 62kΩ
0.01μF | 360kΩ

PACKAGE DIMENSIONS

(Unit: mm)

TQFP80-P-1212-0.50-K



LAPIS Semiconductor Co., Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Plating (≥5μm)
Package weight (g)	0.40 TYP.
Rev. No./Last Revised	1/Feb. 1, 2008

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9473-01	Dec. 15, 2006	–	–	Preliminary edition 1
PEDL9473-02	Jan. 15, 2007	–	–	Preliminary edition 2
PEDL9473-03	Jan. 9, 2008	–	–	Preliminary edition 3
FEDL9473-01	Aug. 21, 2008	–	–	Final edition 1

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