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ON Semiconductor®

# FDMA6023PZT

## Dual P-Channel PowerTrench® MOSFET

-20 V, -3.6 A, 60 mΩ

### Features

- Max  $r_{DS(on)}$  = 60 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -3.6$  A
- Max  $r_{DS(on)}$  = 80 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -3.0$  A
- Max  $r_{DS(on)}$  = 110 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -2.0$  A
- Max  $r_{DS(on)}$  = 170 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -1.0$  A
- Low Profile-0.55 mm maximum - in the new package MicroFET 2x2 mm Thin
- HBM ESD protection level > 2.4 kV typical (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



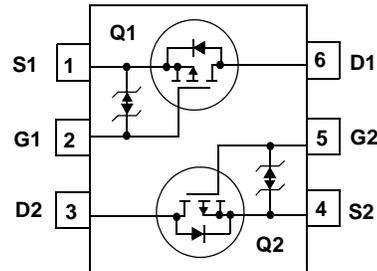
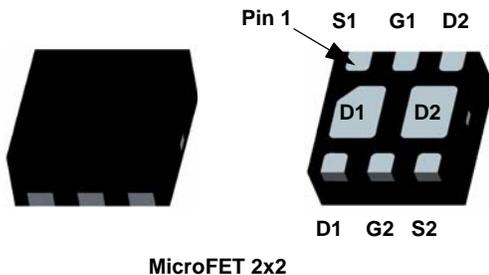
### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultraportable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET 2X2 Thin package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Applications

- Battery protection
- Battery management
- Load switch



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	-Continuous $T_A = 25$ °C (Note 1a)	-3.6	A
	-Pulsed	-15	
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	1.4	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c)	69	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d)	151	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
623	FDMA6023PZT	MicroFET 2X2 Thin	7"	8mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-2.7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$ , $I_D = -3.6\text{ A}$		40	60	m $\Omega$
		$V_{GS} = -2.5\text{ V}$ , $I_D = -3.0\text{ A}$		49	80	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -2.0\text{ A}$		60	110	
		$V_{GS} = -1.5\text{ V}$ , $I_D = -1.0\text{ A}$		70	170	
		$V_{GS} = -4.5\text{ V}$ , $I_D = -3.6\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		58	72	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\text{ V}$ , $I_D = -3.6\text{ A}$		15		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		665	885	pF
$C_{oss}$	Output Capacitance			115	155	pF
$C_{rss}$	Reverse Transfer Capacitance			100	150	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$ , $I_D = -3.6\text{ A}$ , $V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		13	23	ns
$t_r$	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			75	120	ns
$t_f$	Fall Time			47	75	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } -4.5\text{ V}$		12	17
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -10\text{ V}$ , $I_D = -3.6\text{ A}$		1.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.2		nC

**Drain-Source Diode Characteristics**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.1	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -1.1\text{ A}$ (Note 2)		-0.7	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -3.6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
$Q_{rr}$	Reverse Recovery Charge			15	27	nC

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

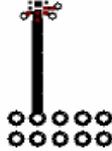
Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  oz. copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

- (a)  $R_{\theta JA} = 86\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper,  $1.5 \times 1.5 \times 0.062\text{ in.}$  thick PCB. For single operation.
- (b)  $R_{\theta JA} = 173\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For single operation.
- (c)  $R_{\theta JA} = 69\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper,  $1.5 \times 1.5 \times 0.062\text{ in.}$  thick PCB. For dual operation.
- (d)  $R_{\theta JA} = 151\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For dual operation.



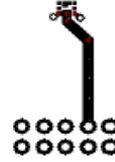
a)  $86\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b)  $173\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.



c)  $69\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.

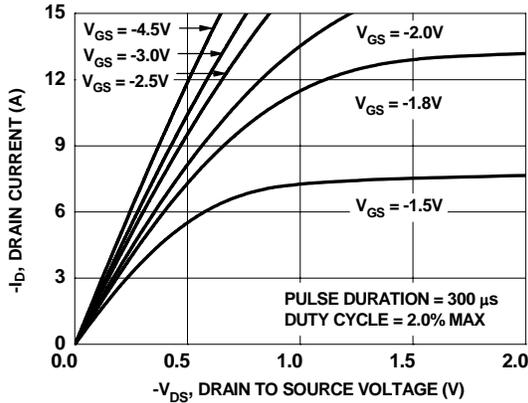


d)  $151\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

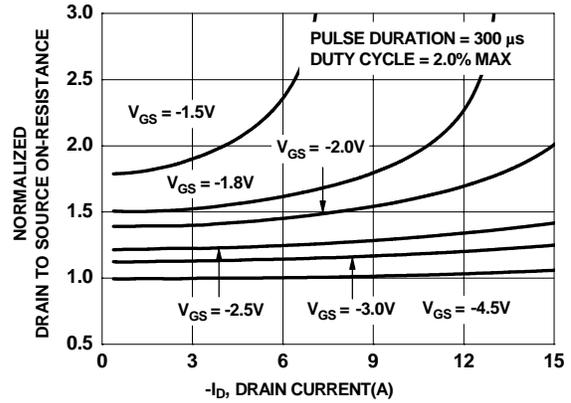
2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

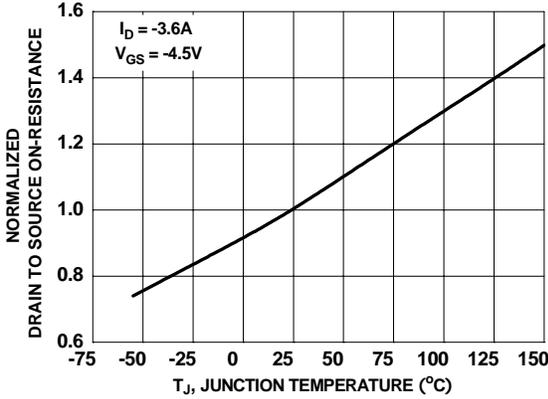
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



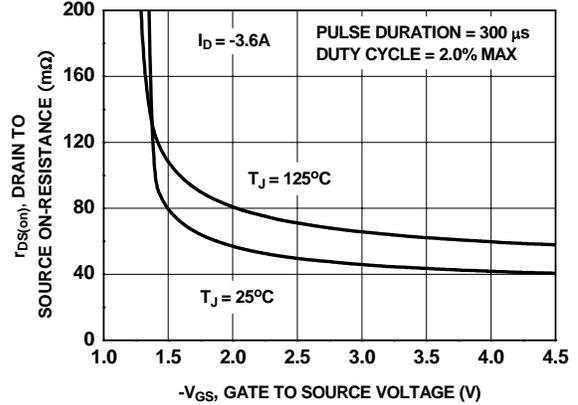
**Figure 1. On-Region Characteristics**



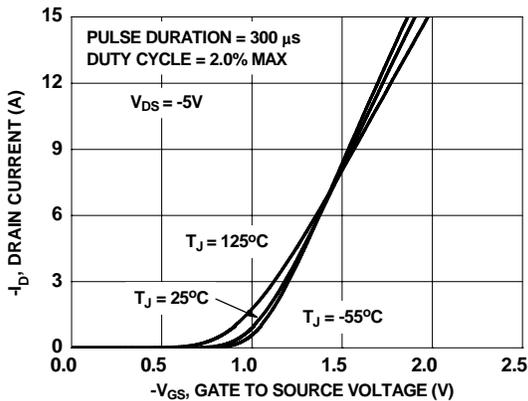
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



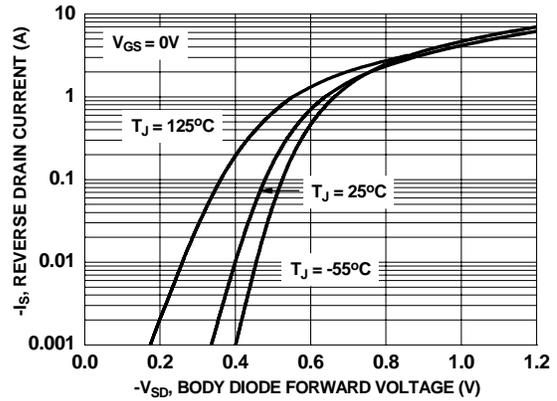
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

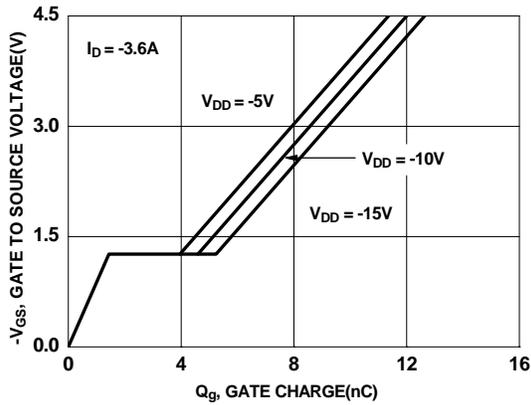


**Figure 5. Transfer Characteristics**

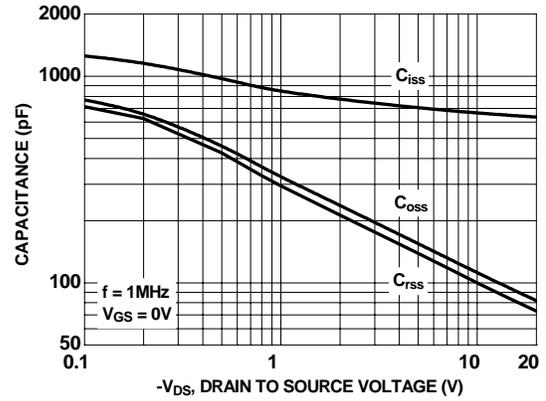


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

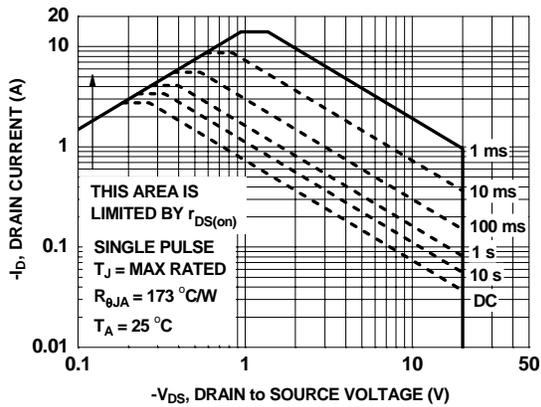
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



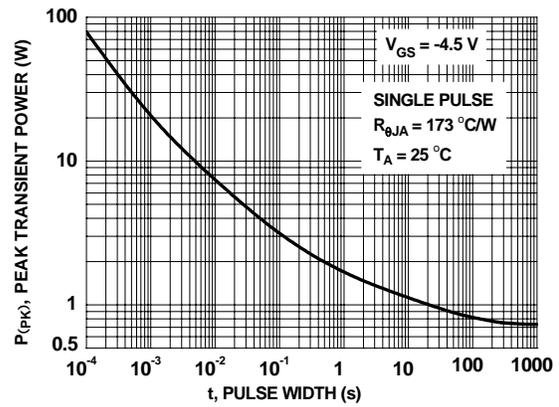
**Figure 7. Gate Charge Characteristics**



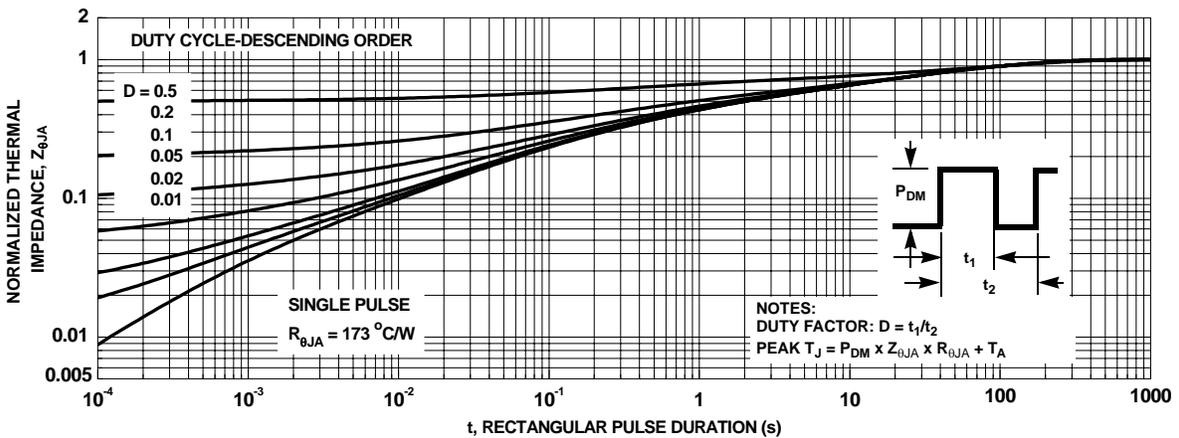
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operation Area**

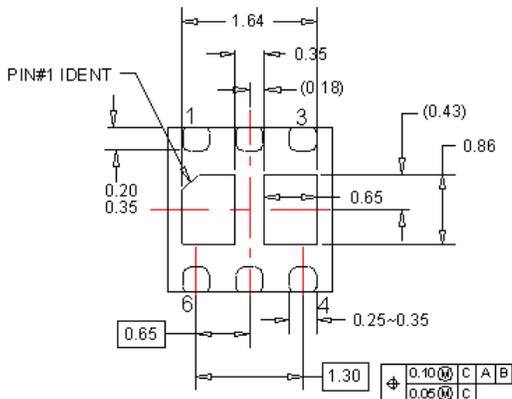
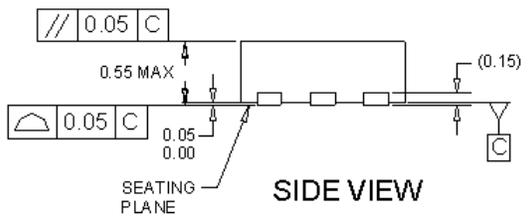
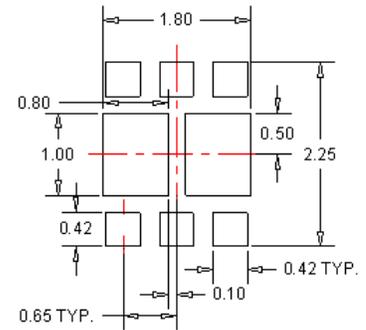
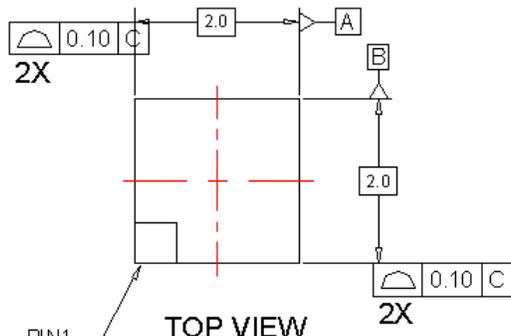


**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



### NOTES:

- A. NO JEDEC STANDARD APPLIES
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILENAME: MKT-UMLP06Brev 1.

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