FAIRCHILD SEMICONDUCTOR®

July 2007

# FDZ7296

## 30V N-Channel PowerTrench® BGA MOSFET

### General Description

Combining Fairchild's advanced PowerTrench process with state-of-the-art BGA packaging, the FDZ7296 minimizes both PCB space and $R_{DS(ON)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

### Applications

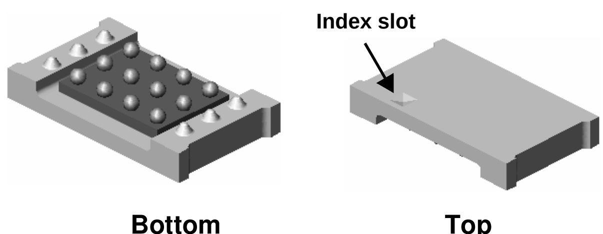
- High-side Mosfet in DC-DC converters for Server and Notebook applications
- RoHS Compliant

### Features

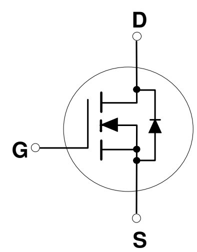
11 A, 30 V. $R_{DS(ON)}$ = 8.5 mΩ @ $V_{GS}$ = 10 V

$R_{DS(ON)}$ = 12 mΩ @ $V_{GS}$ = 4.5 V

- Occupies only 0.10 cm$^2$ of PCB area: 1/3 the area of SO-8.
- Ultra-thin package: less than 0.80 mm height when mounted to PCB.
- High performance trench technology for extremely low $R_{DS(ON)}$
- Optimized for low Qg and Qgd to enable fast switching and reduce CdV/dt gate coupling




BGA 2.5X4.0




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 11 | A |
| | – Pulsed | | 20 | |
| $P_D$ | Power Dissipation (Steady State) | (Note 1a) | 2.1 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 60 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Ball | (Note 1) | 6.3 | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 0.6 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| 7296 | FDZ7296 | 7” | 8mm | 3000 units |

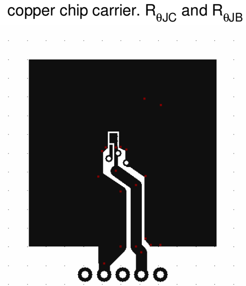
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

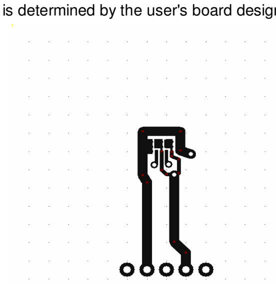
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 27 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| $I_{GSS}$ | Gate–Body Leakage. | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | –4.9 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 11 A<br>$V_{GS}$ = 4.5V, $I_D$ = 10 A<br>$V_{GS}$ = 10 V, $I_D$ = 11 A, $T_J$=125°C | | 7<br>9<br>9.1 | 8.5<br>12<br>13 | mΩ |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1520 | | pF |
| $C_{oss}$ | Output Capacitance | | | 420 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 130 | | pF |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 11 A | | 46 | | S |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 1.1 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 10 | 20 | ns |
| $t_r$ | Turn–On Rise Time | | | 4 | 8 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 27 | 43 | ns |
| $t_f$ | Turn–Off Fall Time | | | 13 | 23 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at Vgs=10V | $V_{DD}$ = 15 V, $I_D$ = 11 A, | | 22 | 31 | nC |
| $Q_g$ | Total Gate Charge at Vgs=5V | | | 12 | 17 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 4.5 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 3.1 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 1.7 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.7 A (Note 2) | | 0.7 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 11A, $d_{iF}/d_t$ = 100 A/µs (Note 2) | | 28 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 18 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 60°C/W when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

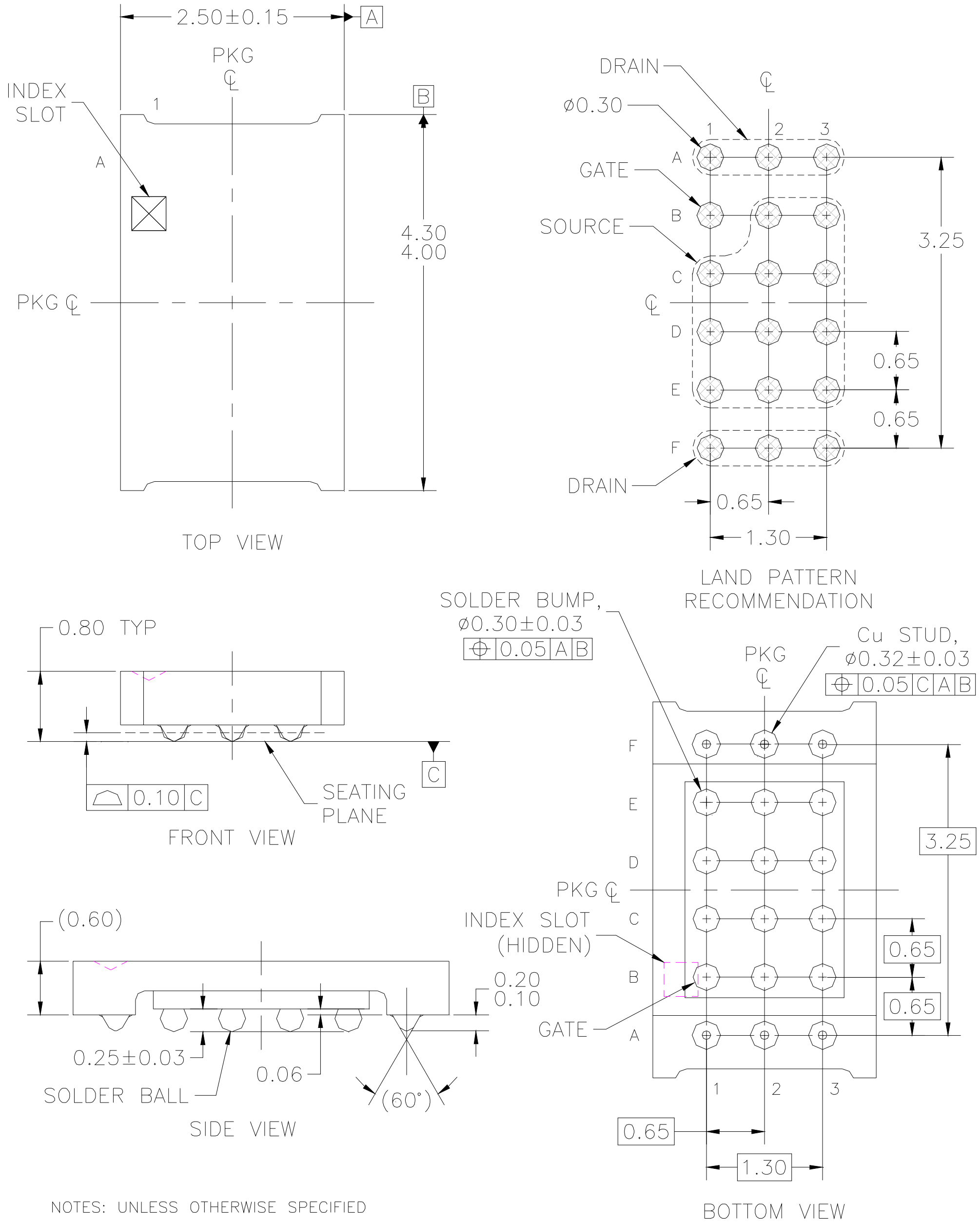


b) 108°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Dimensional Outline and Pad Layout




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.

C) BALL CONFIGURATION TABLE

| TERMINAL | DESIGNATION |
|---|---|
| A1,A2,A3,F1,F2,F3 | DRAIN |
| B1 | GATE |
| B2,B3,C1,C2,C3, D1,D2,D3,E1,E2,E3 | SOURCE |

## Typical Characteristics

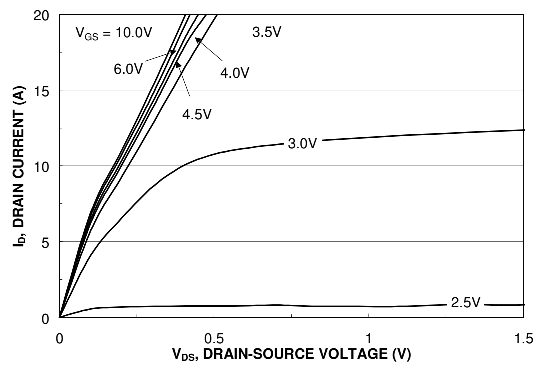



**Figure 1. On-Region Characteristics.**

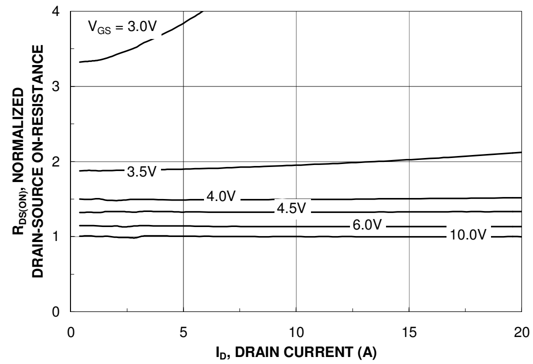



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

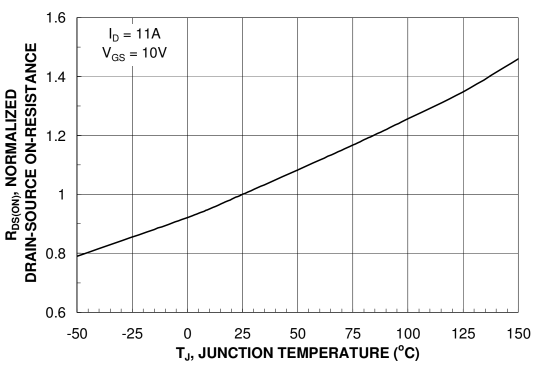



**Figure 3. On-Resistance Variation with Temperature.**

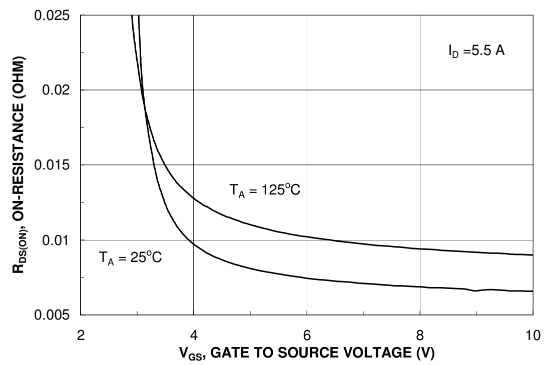



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

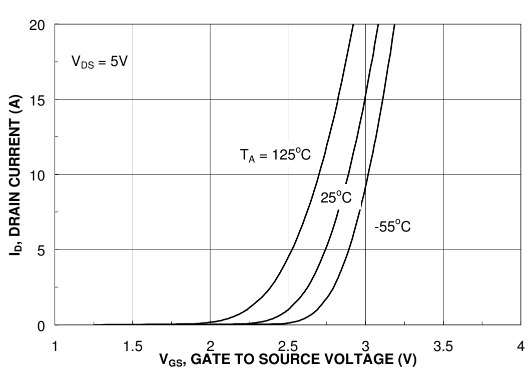



**Figure 5. Transfer Characteristics.**

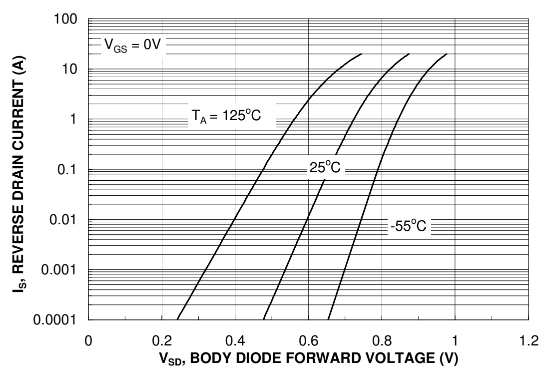



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

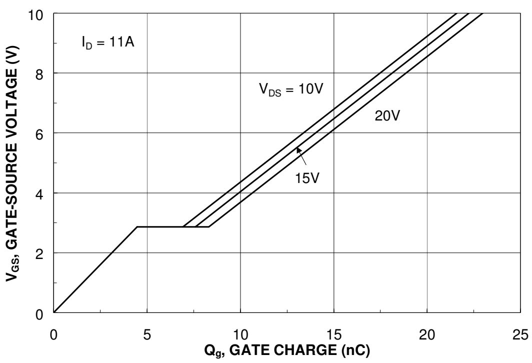



**Figure 7. Gate Charge Characteristics.**

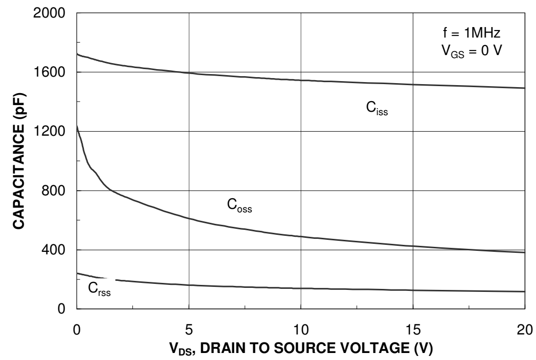



**Figure 8. Capacitance Characteristics.**

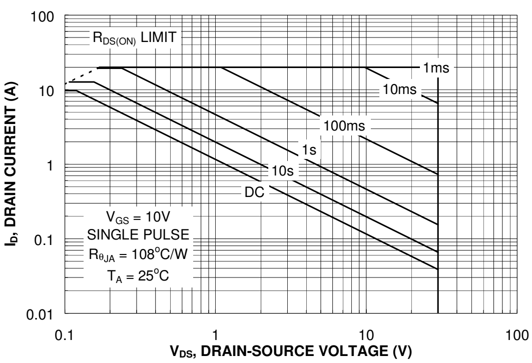



**Figure 9. Maximum Safe Operating Area.**

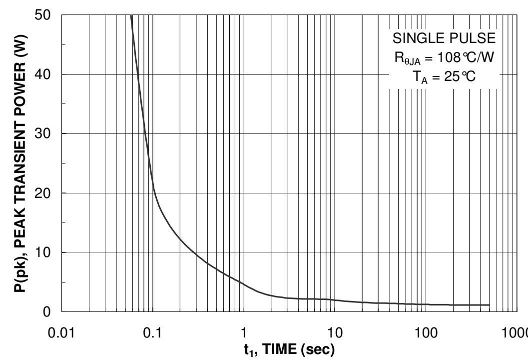



**Figure 10. Single Pulse Maximum Power Dissipation.**

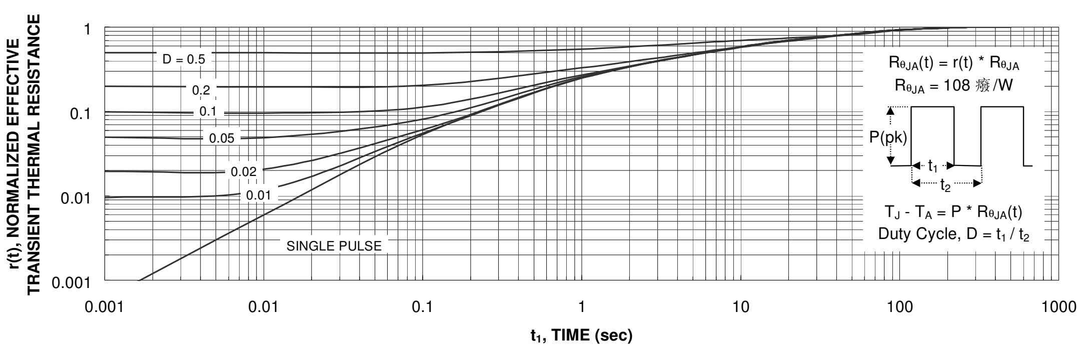



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1b.**
**Transient thermal response will change depending on the circuit board design.**

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