# 75 $\Omega$ Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

#### Rev. V4

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#### Features

- 75 Ω Impedance
- Integrated TTL/CMOS Compatible Driver
- Parallel & Serial (P/S) Control with power-up state selection
- 0.5-dB Attenuation Steps to 31.5 dB
- Low DC Power Consumption
- Lead-Free 4 mm PQFN-24LD Plastic Package
- Halogen-Free "Green" Mold Compound
- RoHS\* Compliant and 260°C Re-flow Compatible

#### Description

The MAAD-008866 is a 6-bit, 0.5-dB step GaAs digital attenuator in a lead-free 4 mm PQFN-24LD surface mount plastic package.

This device is ideally suited for use where high accuracy, very low power consumption and low intermodulation products are required. This part can be used in all 75  $\Omega$  systems operating up to 1.218 GHz.

### **Functional Schematic<sup>3</sup>**



3. Blocking capacitors are required on all RF ports

### **Pin Configuration**

| Pin #  | Function                    | Pin # | Function            |
|--------|-----------------------------|-------|---------------------|
| 1      | Parallel / Serial<br>Select | 16    | Power Up State 2    |
| 2      | Clock                       | 17    | Power Up State 1    |
| 3      | Serial Data In              | 18    | Bias Voltage        |
| 4      | Latch Enable                | 19    | В5                  |
| 5      | Ground                      | 20    | B4                  |
| 6      | RF Input                    | 21    | В3                  |
| 7 - 12 | RF Ground                   | 22    | B2                  |
| 13     | RF Output                   | 23    | B1                  |
| 14     | No Connection               | 24    | В0                  |
| 15     | Serial Data Out             | 25    | Paddle <sup>4</sup> |

The exposed pad centered on the package bottom must be connected to the RF and DC ground.

MAAD-008866-001SMB Sample Board

1. Reference Application Note M513 for reel size information.

2. All sample boards include 5 loose parts.

**Ordering Information**<sup>1,2</sup>

Part Number

MAAD-008866-TR3000

\* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Package

3000 piece reel

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## 75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

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# Electrical Specifications <sup>5,6</sup>: $T_A = 25^{\circ}C$ , $Z_0 = 75 \Omega$ , $V_{DD} = 5 V$ , $V_C = 5 V$

| Parameter                             | Test Conditions  | Units     | Min.         | Тур.                      | Max.          |
|---------------------------------------|--|-----------|--------------|---------------------------|---------------|
| Reference Insertion Loss              | 5 MHz<br>50 MHz<br>500 MHz<br>1000 MHz                   |           | <br>         | 1.3<br>1.35<br>1.6<br>1.8 | <br><br>2.3   |
| Attenuation Accuracy                  | Any Bit or combination<br>5 - 1000 MHz                   | ± (0.15 d | B + 4% of at | ttenuation se             | etting in dB) |
| Return Loss                           | 5 - 1000 MHz   | dB        |              | 18                        | _             |
| T <sub>RISE</sub> , T <sub>FALL</sub> | 10% to 90% RF, 90% to 10% RF                             | ns        | _            | 320                       |               |
| T <sub>ON</sub> , T <sub>OFF</sub>    | 50% Control to 90 / 10% RF                               | ns        | _            | 340                       |               |
| Transients                            | In Band  | mV        | _            | 88                        |               |
| Input P1dB                            | 50 MHz<br>1000 MHz                                       | dBm       | _            | 12<br>25.6                | _             |
| IIP3                                  | 0 dBm/tone at Input, 6 MHz Spacing<br>50 MHz<br>1000 MHz | dBm       |              | 33<br>43                  |               |
| IIP2                                  | 0 dBm/tone at Input, 6 MHz Spacing<br>50 MHz<br>1000 MHz | dBm       | _            | 51<br>74                  | _             |
| Composite Triple Beat, CTB            | 132 channels, +30 dBmV/channel at the input              | dBc       |              | -88                       | _             |
| Composite Second Order, CSO           | 132 channels, +30 dBmV/channel at the input              | dBc       |              | -69                       | _             |
| Steady State I <sub>DD</sub>          | V <sub>DD</sub> = +5 V                                   | μA        | _            | 4                         | —             |

5. External DC blocking capacitors are required on all RF ports. Loss varies at 0.003 dB/°C.

6. Low frequency is determined by DC block and RF GND capacitor value.

## Absolute Maximum Ratings<sup>7,8</sup>

| Parameter                         | Absolute Maximum                                    |
|-----------------------------------|---|
| Input Power<br>50 MHz<br>1000 MHz | +15 dBm<br>+27 dBm                                  |
| Operating Voltage                 | +8.5 V  |
| Control Voltage                   | -0.5 V <u>&lt;</u> V <sub>C</sub> <u>&lt;</u> 5.5 V |
| Operating Temperature             | -40°C to +85°C                                      |
| Storage Temperature               | -65°C to +150°C                                     |

7. Exceeding any one or combination of these limits may cause permanent damage to this device.

8. MACOM does not recommend sustained operation near these survivability limits.

## Truth Table<sup>9</sup>

| B5 | B4 | B3 | B2 | B1 | B0 | Attenuation (dB) |
|----|----|----|----|----|----|------------------|
| 1  | 1  | 1  | 1  | 1  | 1  | Reference IL     |
| 1  | 1  | 1  | 1  | 1  | 0  | 0.5              |
| 1  | 1  | 1  | 1  | 0  | 1  | 1                |
| 1  | 1  | 1  | 0  | 1  | 1  | 2                |
| 1  | 1  | 0  | 1  | 1  | 1  | 4                |
| 1  | 0  | 1  | 1  | 1  | 1  | 8                |
| 0  | 1  | 1  | 1  | 1  | 1  | 16               |
| 0  | 0  | 0  | 0  | 0  | 0  | 31.5             |

9. Logic "0" = 0 to +0.8 V, Logic "1" = +2 to +5 V.

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<sup>2</sup> 



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### **Recommended PCB**



# Application<sup>10</sup>



10.Capacitors C3 - C8 should be as close to package pins as possible.

#### **Off-Chip Component Values**

| Component | Value  | Package |
|-----------|--------|---------|
| C1 & C2   | 0.1 µF | 0402    |
| C3 - C8   | 0.1 µF | 0201    |

#### **Handling Procedures**

Please observe the following precautions to avoid damage:

#### **Static Sensitivity**

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. An external protection circuit using an inexpensive anti-parallel diode pair can be used to protect the IC.

Please reference application note AN3028 for further detail.

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### **Typical Performance Curves**

#### Insertion Loss



Input Return Loss, across all attenuation states



Relative Attenuation across all major states



Output Return Loss, across all attenuation states



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### Typical Performance Curves @ 5 Volts

#### Step Error vs. State over Frequency



Step Error vs. State over Temp @ 500 MHz



Step Error vs. State over Temp @ 5 MHz



Step Error vs. State over Temp @ 1000 MHz



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# 75 $\Omega$ Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

## Typical Performance Curves @ 5 Volts

#### IIP3 vs. Frequency @ 25°C



IIP3 vs. Frequency @ -40°C



IIP3 vs. Frequency @ +85°C



IIP2 vs. Frequency @ 25°C



#### IIP2 vs. Frequency @ -40°C



IIP2 vs. Frequency @ +85°C



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## 75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

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## Functionality Modes of Operation: Serial, Direct Parallel, and Latched Parallel

### Mode Truth Table

| P/S | LE            | Mode             |
|-----|---------------|------------------|
| 1   | Х             | Serial           |
| 0   | Constant High | Direct Parallel  |
| 0   | Pulsed        | Latched Parallel |

#### Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with MSB first. After shifting in the 6 bit word, bringing LE high will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change . SEROUT is the SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled and the serial input register is loaded asynchronously with parallel digital inputs.

#### Direct Parallel Mode

The parallel mode is enabled when P/S is set to low. In the direct parallel mode, the attenuator is controlled by the parallel control inputs directly. The LE must be at logic high to control the attenuator in this mode.

#### Latched Parallel Mode

In the latched parallel mode, the parallel control inputs will be buffered by registers, and loaded to the outputs when LE is high. The outputs shall not change states when LE is low.

#### **Power-up States**

The power-up (PUP) states will work in both serial and parallel modes, and initiate the attenuator according to the PUP truth table. During power up, the digital inputs shall be held constant for at least 1  $\mu$ s after V<sub>DD</sub> reaches 90% of final value. For serial mode, the PUP states will only work when LE is held low. The PUP state shall be locked out after the first LE pulse.

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## 75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

## Functionality Modes of Operation: Serial, Direct Parallel, and Latched Parallel

|    | Inp | uts  |      |                                  |             |
|----|-----|------|------|----------------------------------|-------------|
| PS | LE  | PUP2 | PUP1 | Gain Relative to Max. Gain       | Notes       |
| 0  | 0   | 0    | 0    | -31.5 dB                         |             |
| 0  | 0   | 0    | 1    | -24 dB                           |             |
| 0  | 0   | 1    | 0    | 0 -16 dB                         |             |
| 0  | 0   | 1    | 1    | Insertion Loss                   |             |
| 0  | 1   | Х    | Х    | 0 to -31.5 dB (Set VC0.5 - VC16) |             |
| 1  | 0   | Х    | Х    | 0 to -31.5 dB (Set VC0.5 - VC16) | Sorial Mada |
| 1  | 1   | Х    | Х    | No Definition                    | Serial Mode |

### **PUP Truth Table\***

 $V_{DD} T_{RISE}$  must be <= 125 ns

### **Serial Interface Timing Characteristics**

| Symbol           | Parameter                           | т     | Units |       |       |
|------------------|-------------------------------------|-------|-------|-------|-------|
| Symbol           | Parameter                           | -40°C | 25°C  | +85°C | Units |
| t <sub>scк</sub> | Min. Serial Clock Period            | 100   | 100   | 100   | ns    |
| t <sub>cs</sub>  | Min. Control Set-up Time            | 20    | 20    | 20    | ns    |
| t <sub>сн</sub>  | Min. Control Hold Time              | 20    | 20    | 20    | ns    |
| t <sub>LS</sub>  | Min. LE Set-up Time                 | 10    | 10    | 10    | ns    |
| t <sub>LEW</sub> | Min. LE Pulse Width                 | 10    | 10    | 10    | ns    |
| t <sub>LH</sub>  | Min. Serial Clock Hold Time from LE | 10    | 10    | 10    | ns    |
| t <sub>LES</sub> | Min. LE Pulse Spacing               | 630   | 630   | 630   | ns    |

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Functionality Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Serial Input Interface Timing Diagram



### **Parallel Control Word**



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## 75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

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## Lead Free 4 mm 24-Lead PQFN <sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements. Plating is 100% matte tin over copper.

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## 75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

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#### 5 - 1218 MHz Application Section

# Electrical Specifications<sup>5,6</sup>: $T_A = 25^{\circ}C$ , $Z_0 = 75 \Omega$ , $V_{DD} = 5 V$ , $V_C = 5 V$

| Parameter                             | Test Conditions  | Units     | Min.         | Тур.                             | Max.            |
|---------------------------------------|--|-----------|--------------|----------------------------------|-----------------|
| Reference Insertion Loss              | 5 MHz<br>50 MHz<br>500 MHz<br>1000 MHz<br>1218 MHz       |           |              | 1.3<br>1.35<br>1.6<br>1.8<br>1.9 | <br><br>2.3<br> |
| Attenuation Accuracy                  | Any Bit or combination<br>5 - 1000 MHz                   | ± (0.15 d | IB + 4% of a | ttenuation se                    | etting in dB)   |
| Return Loss                           | 5 - 1218 MHz   | dB        |              | 18                               | _               |
| T <sub>RISE</sub> , T <sub>FALL</sub> | 10% to 90% RF, 90% to 10% RF                             | ns        | _            | 320                              | _               |
| T <sub>ON</sub> , T <sub>OFF</sub>    | 50% Control to 90 / 10% RF                               | ns        | _            | 340                              | _               |
| Transients                            | In Band  | mV        | _            | 88                               | _               |
| Input P1dB                            | 50 MHz<br>1000 MHz                                       | dBm       | —            | 12<br>25.6                       | _               |
| IIP3                                  | 0 dBm/tone at Input, 6 MHz Spacing<br>50 MHz<br>1000 MHz | dBm       |              | 33<br>43                         | _               |
| IIP2                                  | 0 dBm/tone at Input, 6 MHz Spacing<br>50 MHz<br>1000 MHz | dBm       | _            | 51<br>74                         | _               |
| Composite Triple Beat, CTB            | 132 channels, +30 dBmV/channel at the input              | dBc       |              | -88                              | _               |
| Composite Second Order, CSO           | 132 channels, +30 dBmV/channel at the input              | dBc       | _            | -69                              | _               |
| Steady State I <sub>DD</sub>          | V <sub>DD</sub> = +5 V                                   | μA        | —            | 4                                | —               |

5. External DC blocking capacitors are required on all RF ports. Loss varies at 0.003 dB/°C.

6. Low frequency is determined by DC block and RF GND capacitor value.



10.Capacitors C3 - C8 should be as close to package pins as possible.

#### **Off-Chip Component Values**

| Component | Value  | Package |
|-----------|--------|---------|
| C1 & C2   | 0.1 µF | 0402    |
| C3 - C8   | 0.1 µF | 0201    |



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# 75 $\Omega$ Digital Attenuator, 6-Bit, Serial / Parallel Control 31.5 dB, 0.005 - 1.218 GHz

### 5 - 1218 MHz Application Section

### **Typical Performance Curves**

Insertion Loss



#### Input Return Loss, across all attenuation states



#### Relative Attenuation across all major states



#### Output Return Loss, across all attenuation states



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