800-mA , 3-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER

Check for Samples: TPS62692, TPS62693, TPS62694, TPS62698

FEATURES

- **95% Efficiency at 3MHz Operation**
- **21 µA Quiescent Current**
- **3 MHz Regulated Frequency Operation**
- **Spread Spectrum, PWM Frequency Dithering**
- **High Duty-Cycle Operation**
- **±2% Total DC Voltage Accuracy**
- ***Best in Class* Load and Line Transient**
- **Excellent AC Load Regulation**
- **Low Ripple Light-Load PFM Mode**
- **≥40 dB V_{IN} PSRR (1 kHz to 10 kHz)**
- **Internal Soft Start, 350-µs Start-Up Time**
- **Integrated Active Power-Down Sequencing (Optional)**
- **Current Overload and Thermal Shutdown Protection**
- **Three Surface-Mount External Components Required (One 2012 MLCC Inductor, Two 0402 Ceramic Capacitors)**
- **Complete Sub 1-mm Component Profile Solution**
- **Total Solution Size <12 mm^2 (CSP)**
- **Available in a 6-Pin NanoFree™ (CSP)**

APPLICATIONS

- **Memory Cards**
- **LDO Replacement**
- **Cell Phones, Smart-Phones**
- **WLAN, *Bluetooth*™ Applications**

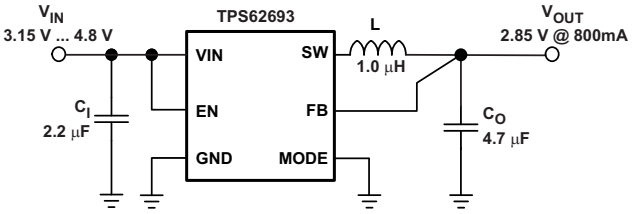

Figure 1. Smallest Solution Size Application

DESCRIPTION

The TPS62693 device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS62693 supports up to 800-mA load current, and allows the use of low cost chip inductor and capacitors.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Li-Ion battery. Different fixed output voltage versions are available in the range from 2.2 V up to 3.3 V.

The TPS62693 operates at a regulated 3-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 21 µA (typical) during light load operation. For noise-sensitive applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. This feature, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

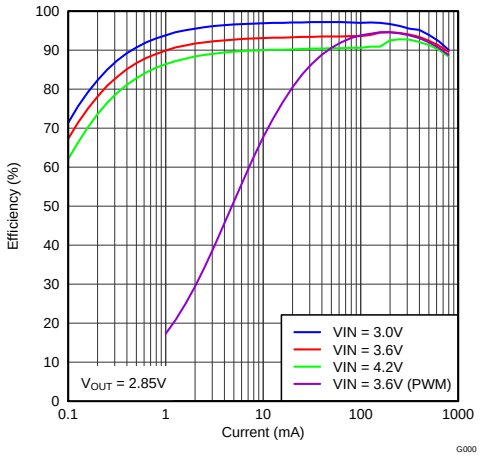

Figure 2. Efficiency vs. Load Current

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Bluetooth is a trademark of Bluetooth SIG.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	DEVICE SPECIFIC FEATURE	ORDERING(3)	PACKAGE MARKING CHIP CODE
-40°C to 85°C	TPS62692	2.2(4)	800 mA peak output current Output Discharge Spread Spectrum Frequency Modulation	TPS62692YFD	TW
-40°C to 85°C	TPS62693	2.85	800 mA peak output current Output Discharge Spread Spectrum Frequency Modulation	TPS62693YFD	UD
-40°C to 85°C	TPS62694	2.95(4)	800 mA peak output current Output Discharge Spread Spectrum Frequency Modulation	TPS62694YFD	B6
-40°C to 85°C	TPS62698	3.0	800 mA peak output current Output Discharge	TPS62698YFD	B7

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Internal tap points are available to facilitate output voltages in 25mV increments.
(3) The YFD package is available in tape and reel. Add a R suffix (e.g. TPS62692YFDR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS62692YFDT) to order quantities of 250 parts.
(4) Product preview. Contact TI factory for more information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	Voltage at VIN(2)(3), SW(3)	–0.3	6	V
	Voltage at FB(4)	–0.3	3.6	V
	Voltage at EN, MODE (3)	–0.3	V_I + 0.3	V
Peak output current, I_O			800(4)	mA
Power dissipation		Internally limited		
Operating temperature range, T_A (5)		–40	85	°C
Operating junction temperature, T_J			150	°C
Storage temperature range, T_{stg}		–65	150	°C
ESD(6)	Human body model		2	kV
	Charge device model		1	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8V input voltage is not recommended over an extended period of time.
(3) All voltage values are with respect to network ground terminal.
(4) Limited to 50% Duty Cycle over Lifetime.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.
(6) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS6269x YFD (6 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	132.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.2	
θ_{JB}	Junction-to-board thermal resistance	22.7	
ψ_{JT}	Junction-to-top characterization parameter	5.7	
ψ_{JB}	Junction-to-board characterization parameter	22.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.3		4.8(1)	V
I_O	Output current range	0		800	mA
L	Inductance	0.5		1.8	µH
C_O	Output capacitance	1	5	10	µF
T_A	Ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Operation above 4.8V input voltage is not recommended over an extended period of time.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current		I_O = 0mA. Device not switching		21	50	µA
			I_O = 0mA, PWM mode		3.5		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	7	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage			1			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance		V_{IN} = $V_{(GS)}$ = 3.6V. PWM mode		165	275	mΩ
			V_{IN} = $V_{(GS)}$ = 2.9V. PWM mode		185	350	mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			6	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		V_{IN} = $V_{(GS)}$ = 3.6V. PWM mode		140	250	mΩ
			V_{IN} = $V_{(GS)}$ = 2.9V. PWM mode		160	330	mΩ
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			6	µA
r_{DIS}	Discharge resistor for power-down sequence				120		Ω
	P-MOS current limit		2.3V ≤ V_{IN} ≤ 4.8V. Open loop	1100	1250	1500	mA
			V_{IN} = 3.6V. Closed loop		900		mA
	Input current limit under short-circuit conditions		V_O shorted to ground		15		mA

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

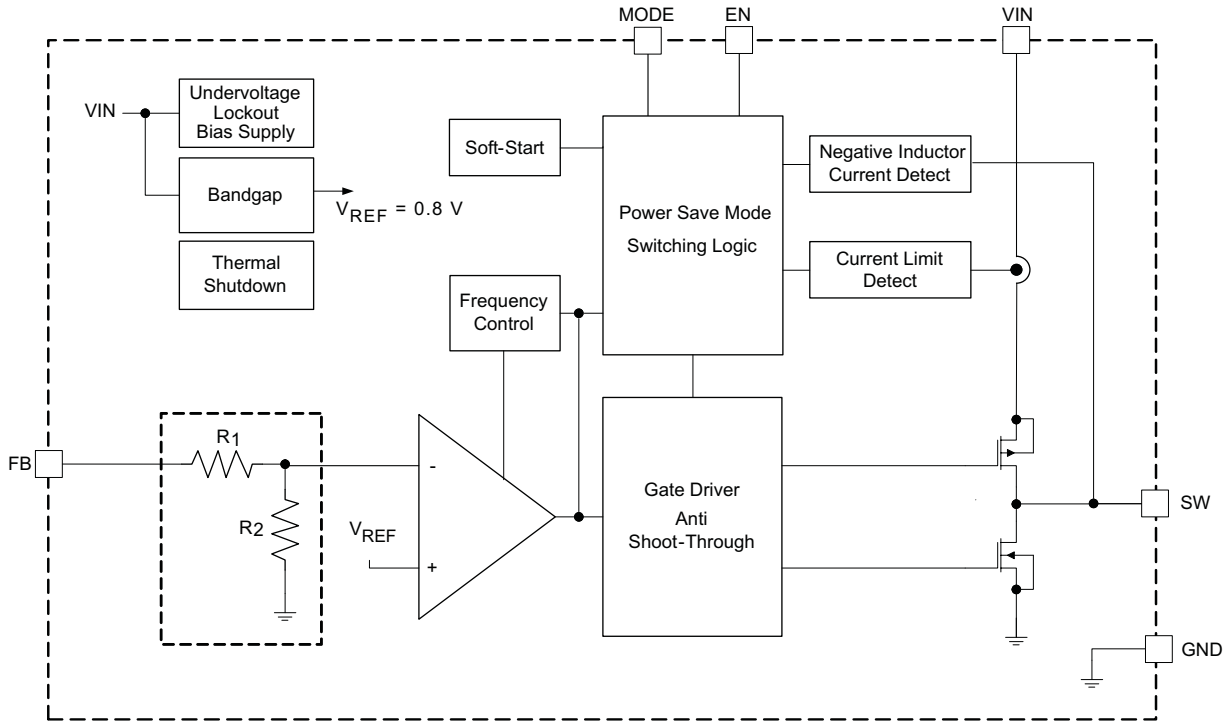
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
OSCILLATOR							
f_{SW}	Oscillator frequency		I_O = 0mA, PWM mode.	2.7	3	3.3	MHz
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS62692	2.65V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.65V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.65V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS62693	3.15V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS62694	3.25V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.25V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.25V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS62698	3.3V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
	Line regulation		V_{IN} = V_O + 0.5V (min 3.3V) to 5.5V I_O = 200 mA		0.18		%/V
	Load regulation		I_O = 0mA to 800 mA		-0.0003		%/mA
	Feedback input resistance				450		kΩ
ΔV_O	Power-save mode ripple voltage	TPS62693 TPS62694 TPS62698	I_O = 1mA C_O = 4.7µF X5R 6.3V 0402		65		mV_{PP}
			I_O = 1mA C_O = 10µF X5R 6.3V 0603		25		mV_{PP}
		TPS62692	I_O = 1mA C_O = 10µF X5R 6.3V 0603		22		mV_{PP}
	Start-up time	TPS6269x	I_O = 0mA, Time from active EN to start switching		60		µs
		TPS62693 TPS62694 TPS62698	I_O = 0mA, Time to ramp from 5% to 95% of VOUT		250		µs
		TPS62692	I_O = 0mA, Time to ramp from 5% to 95% of VOUT		200		µs

PIN ASSIGNMENTS TPS62692

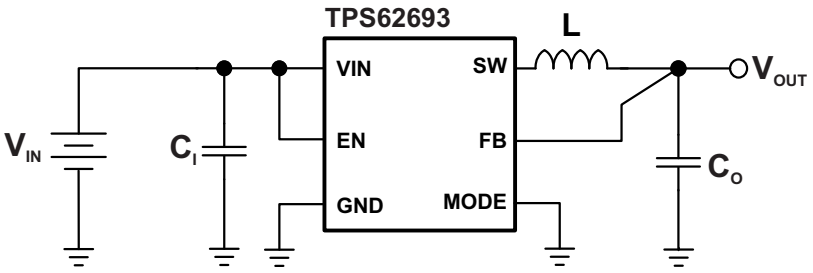
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated. MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C2	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of components:

- L = TOKO MDT2012CR1R0
- C_I = MURATA GRM155R60J225ME15 (2.2µF, 6.3V, 0402, X5R)
- C_O = 2 x MURATA GRM155R60J475ME97 (4.7µF, 6.3V, 0402, X5R)

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS			FIGURE
η	Efficiency	vs Load current (TPS62693, V_{OUT} = 2.85V)	3, 4
		vs Load current (TPS62698, V_{OUT} = 3.0V)	5
		vs Load current (TPS62692, V_{OUT} = 2.2V)	6, 7
		vs Input voltage (TPS62693, V_{OUT} = 2.85V)	8
		vs Input voltage (TPS62692, V_{OUT} = 2.2V)	9
	Peak-to-peak output ripple voltage	vs Load current	10, 11
	Combined line/load transient response		12
	Load transient response	TPS62693, V_{OUT} = 2.85V	13, 14, 15
		TPS62692, V_{OUT} = 2.2V	16, 17
	AC load transient response	TPS62693, V_{OUT} = 2.85V	18, 19
		TPS62692, V_{OUT} = 2.2V	20, 21
V_O	DC output voltage	vs Load current, TPS62693, V_{OUT} = 2.85V (MODE = low)	22
		vs Load current, TPS62692, V_{OUT} = 2.2V (MODE = hi)	23, 24
		vs Load current, TPS62693, V_{OUT} = 2.2V (MODE = low)	25
	PFM/PWM boundaries	vs Input voltage (TPS62693, V_{OUT} = 2.85V)	26
I_Q	Quiescent current	vs Input voltage	27
f_s	PWM switching frequency	vs Input voltage (TPS62693, V_{OUT} = 2.85V)	28
	PFM switching frequency	vs Load current (TPS62693, V_{OUT} = 2.85V)	29
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	30
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	31
	PWM operation	TPS62693, V_{OUT} = 2.85V	32
	Power-save mode operation	TPS62693, V_{OUT} = 2.85V	33
	Spread Spectrum Frequency Modulation	TPS62692, V_{OUT} = 2.2V	34
	Start-up	TPS62693, V_{OUT} = 2.85V	35, 36
	Shut-Down	TPS62693, V_{OUT} = 2.85V	37

TYPICAL CHARACTERISTICS (continued)

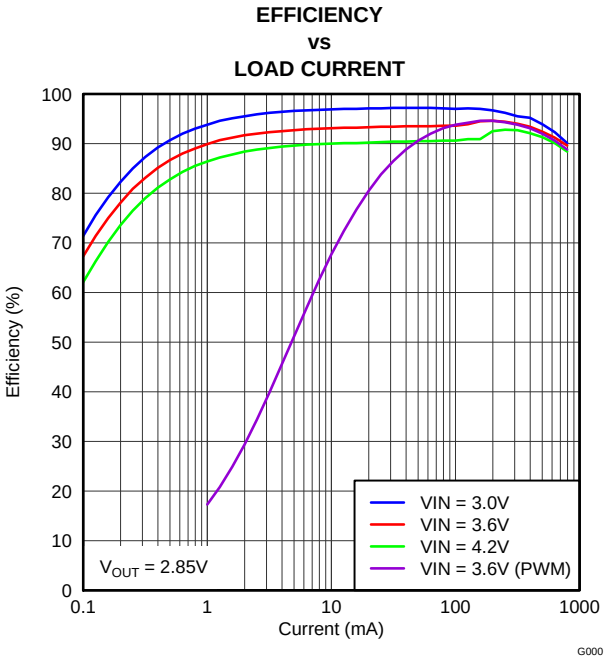


Figure 3.

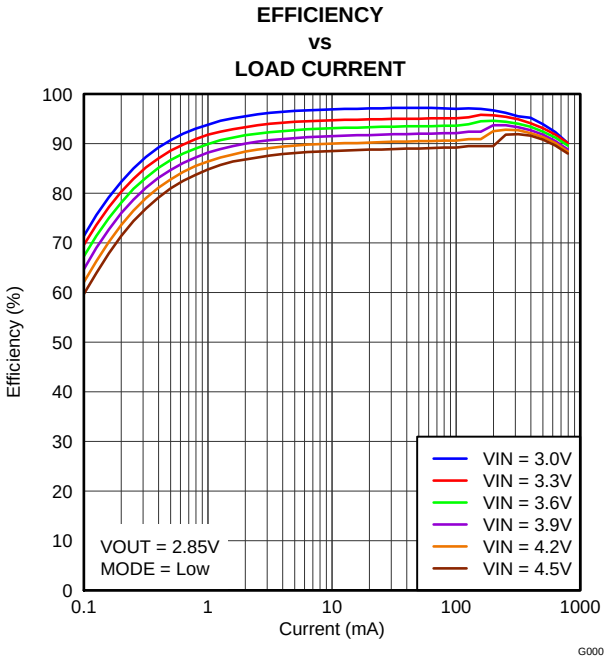


Figure 4.

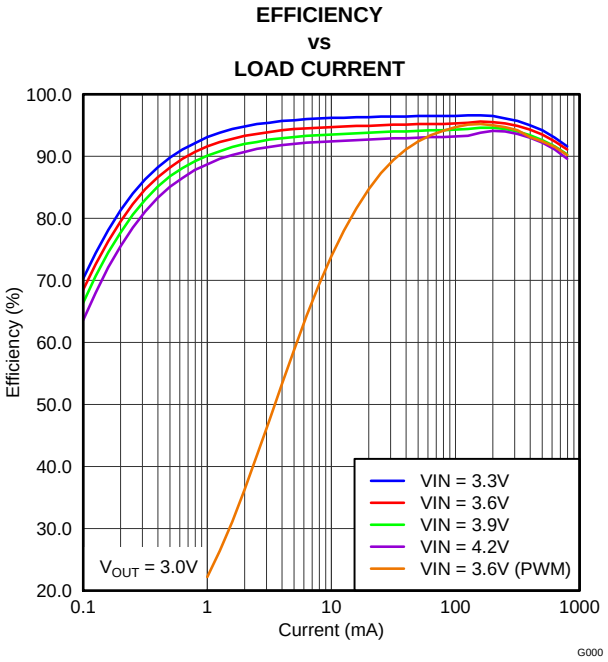


Figure 5.

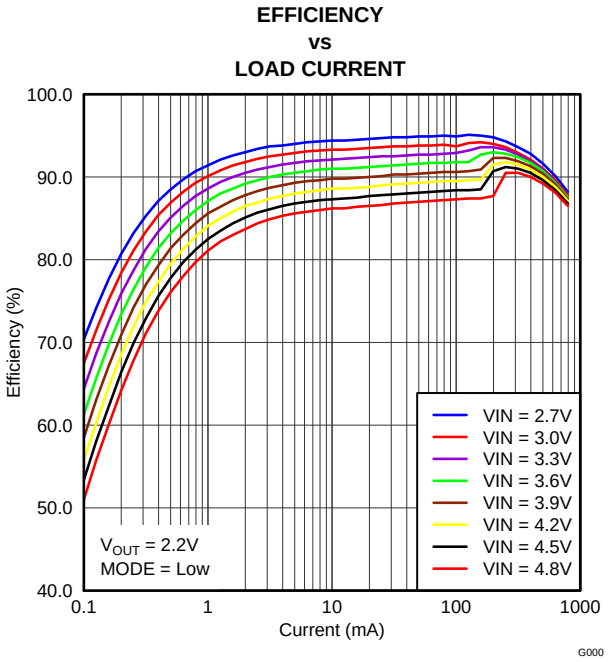


Figure 6.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs LOAD CURRENT

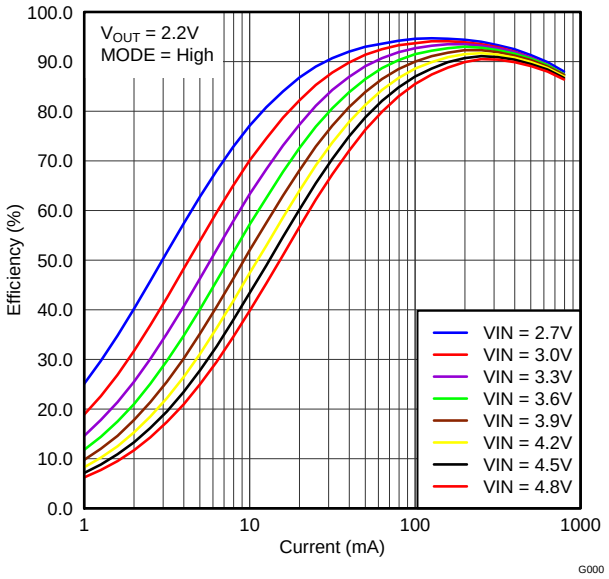


Figure 7.

EFFICIENCY vs INPUT VOLTAGE

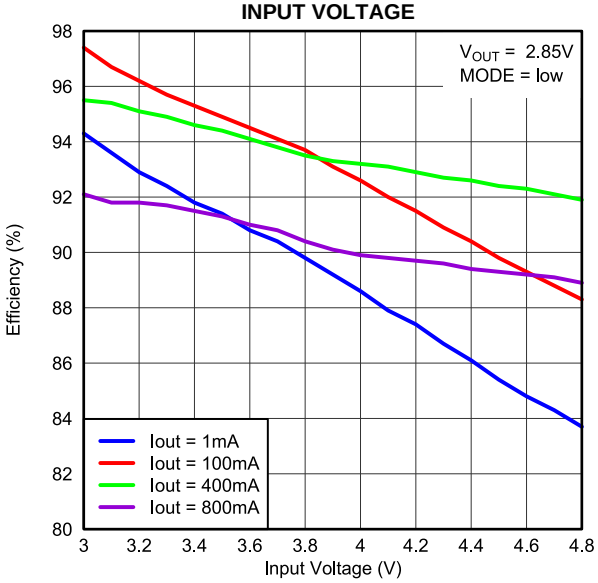


Figure 8.

EFFICIENCY vs INPUT VOLTAGE

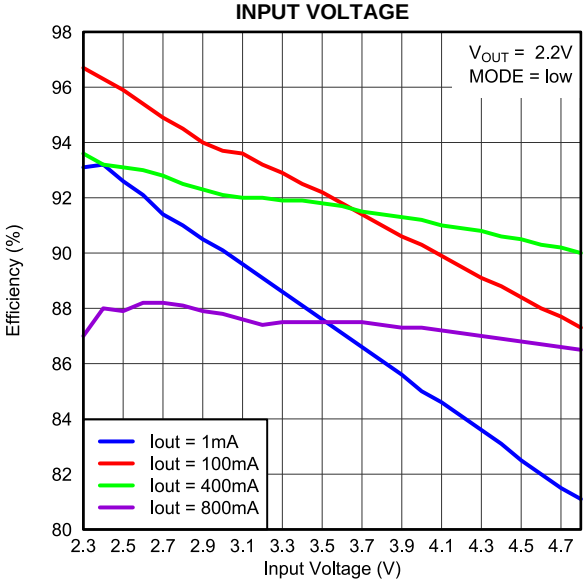


Figure 9.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

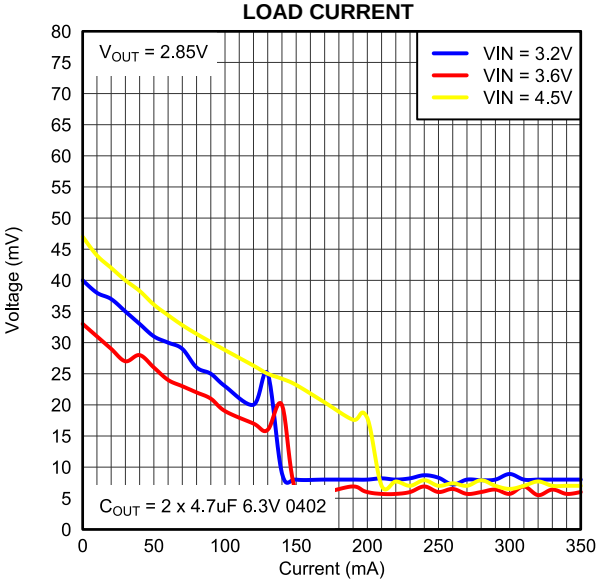


Figure 10.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

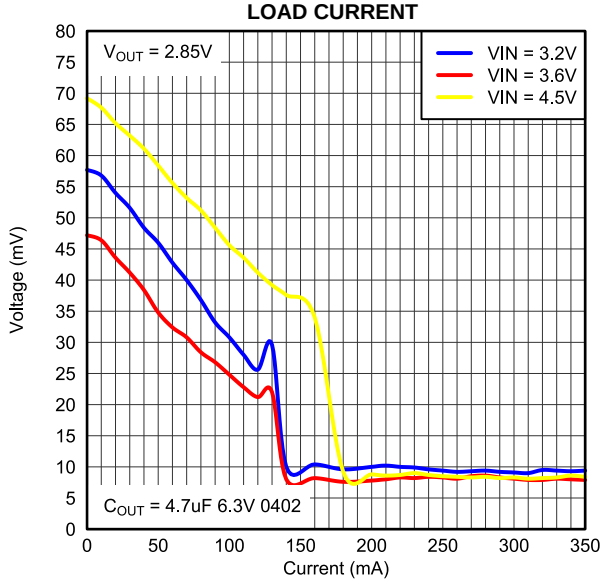


Figure 11.

COMBINED LINE/LOAD TRANSIENT RESPONSE

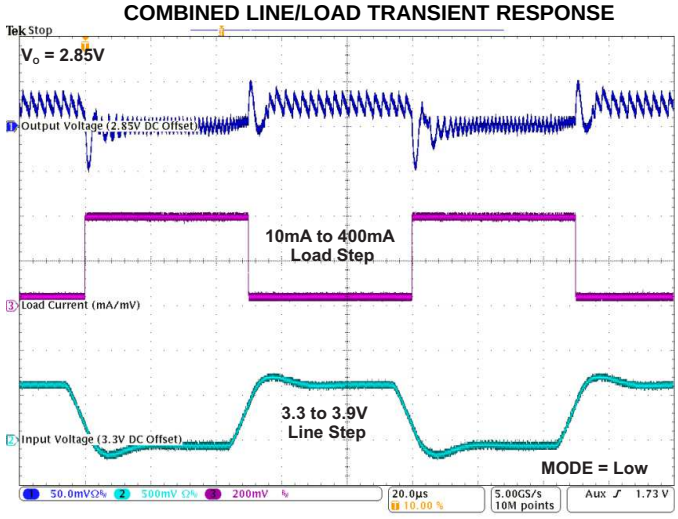


Figure 12.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

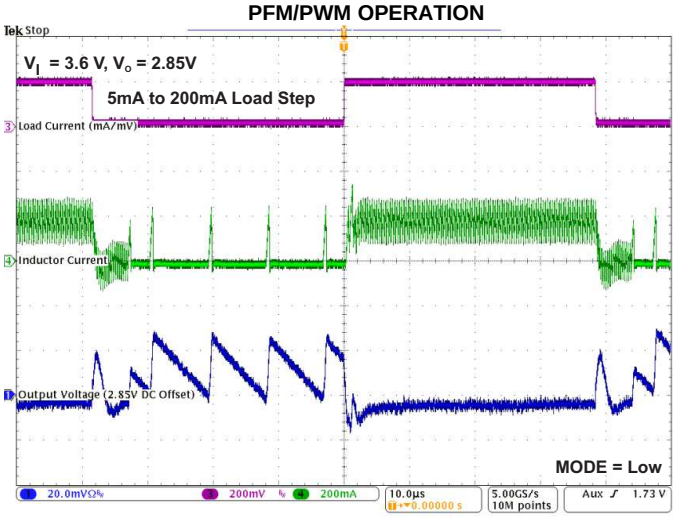


Figure 13.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

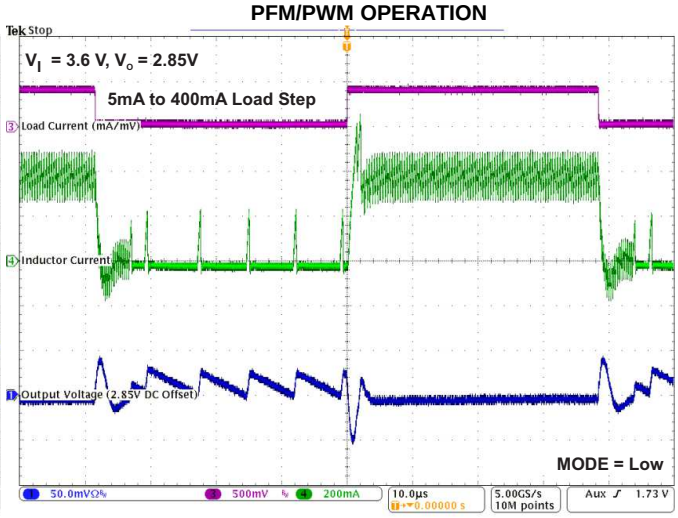


Figure 14.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

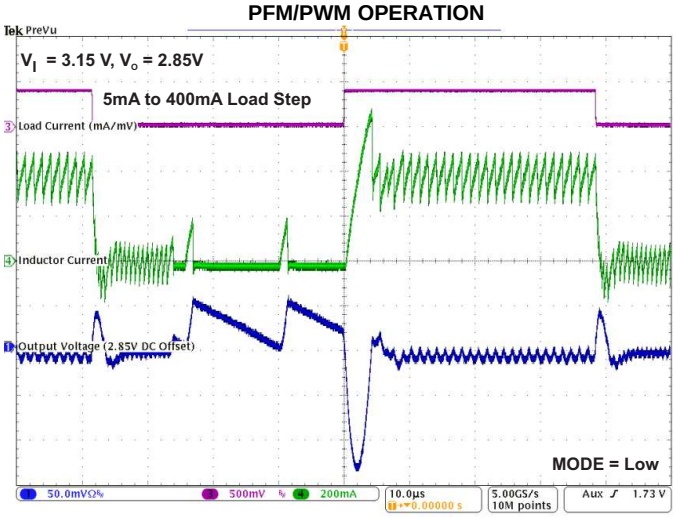


Figure 15.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

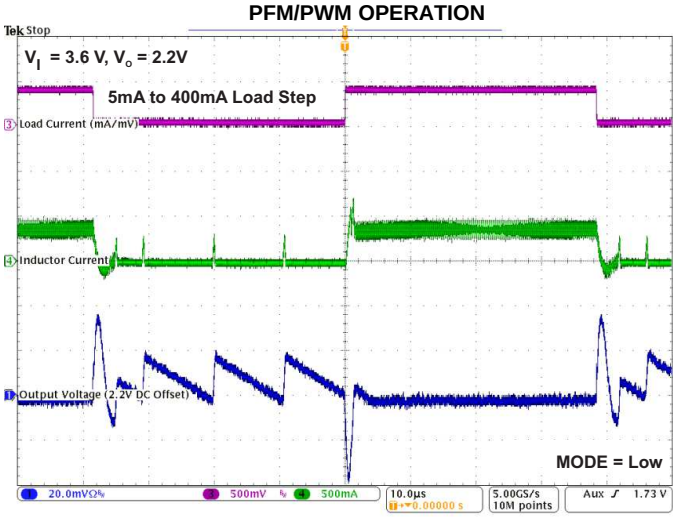


Figure 16.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

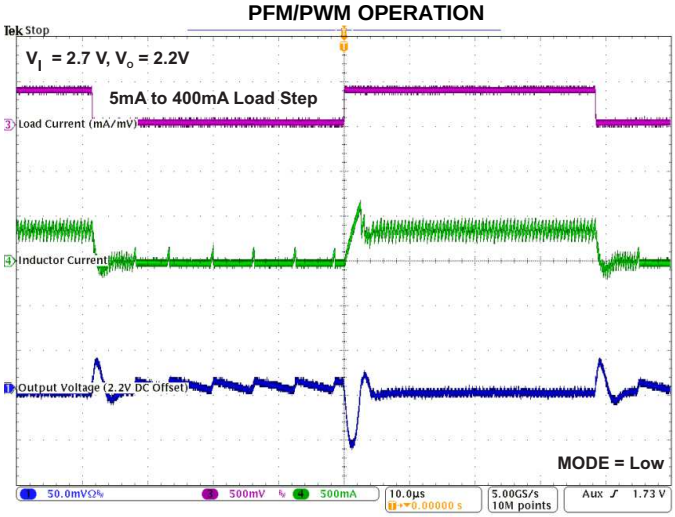


Figure 17.

AC LOAD TRANSIENT RESPONSE

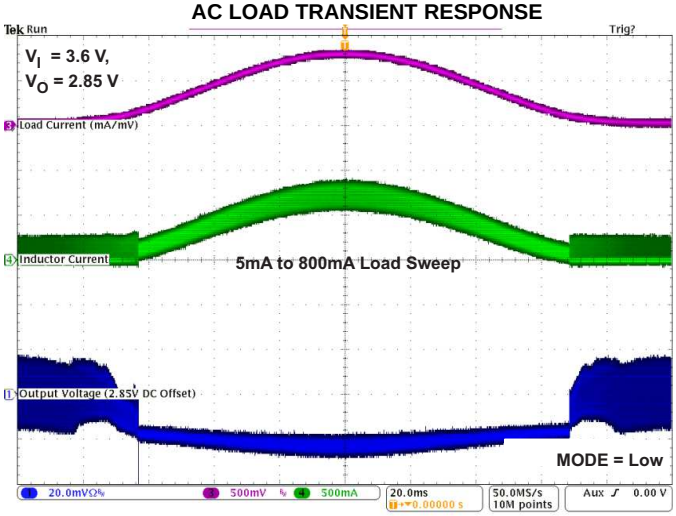


Figure 18.

TYPICAL CHARACTERISTICS (continued)

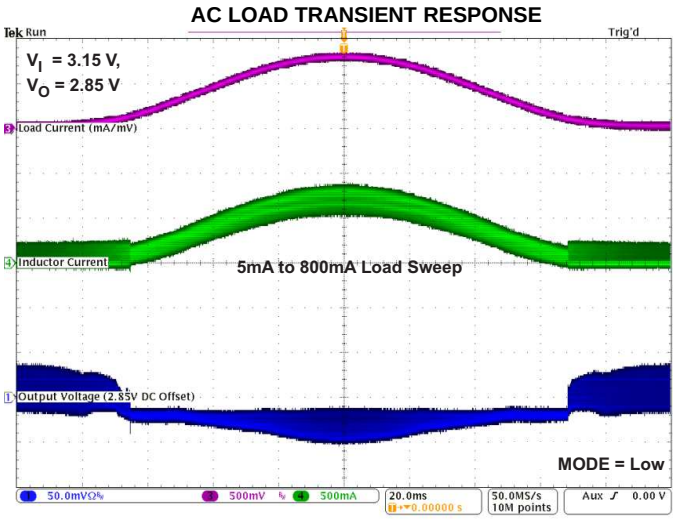


Figure 19.

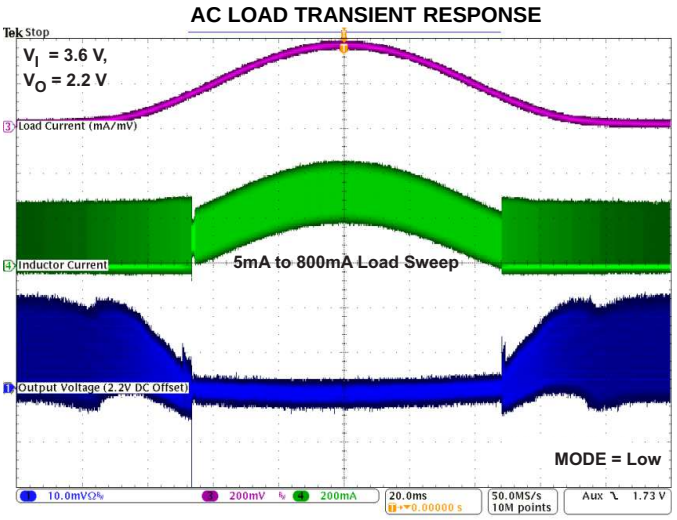


Figure 20.

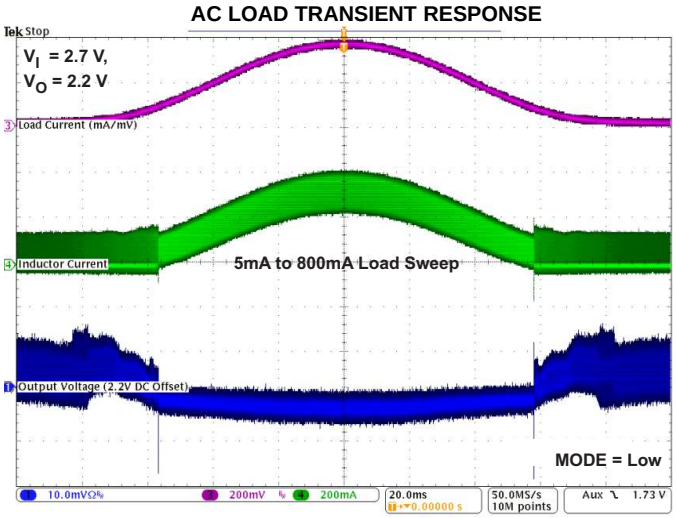


Figure 21.

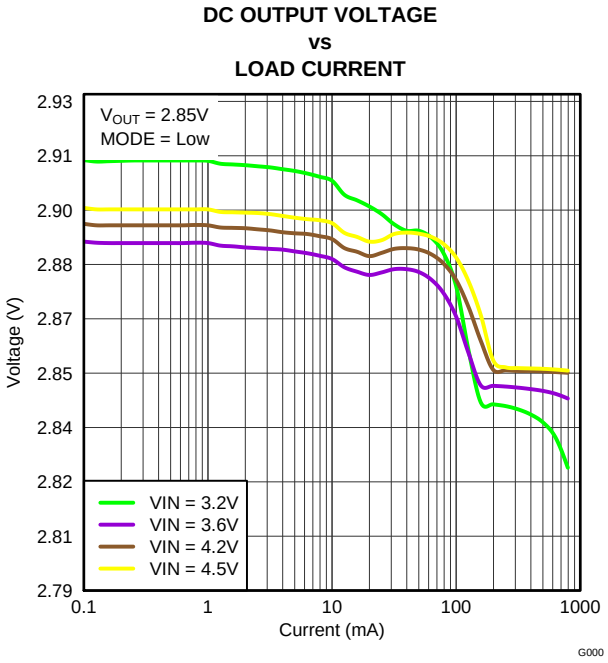


Figure 22.

TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE vs LOAD CURRENT

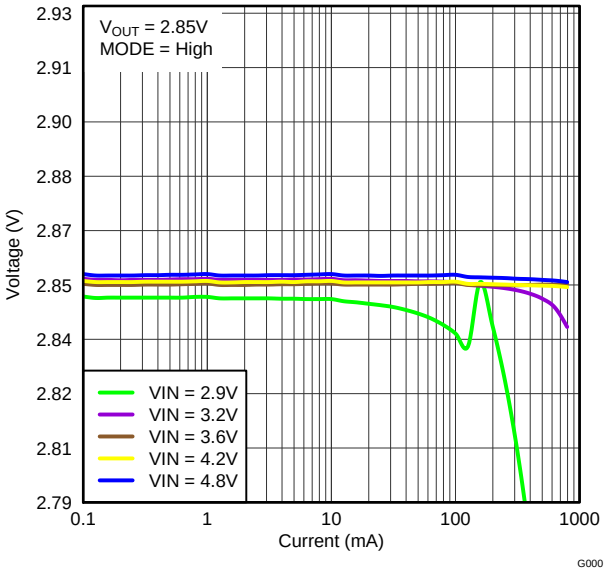


Figure 23.

DC OUTPUT VOLTAGE vs LOAD CURRENT

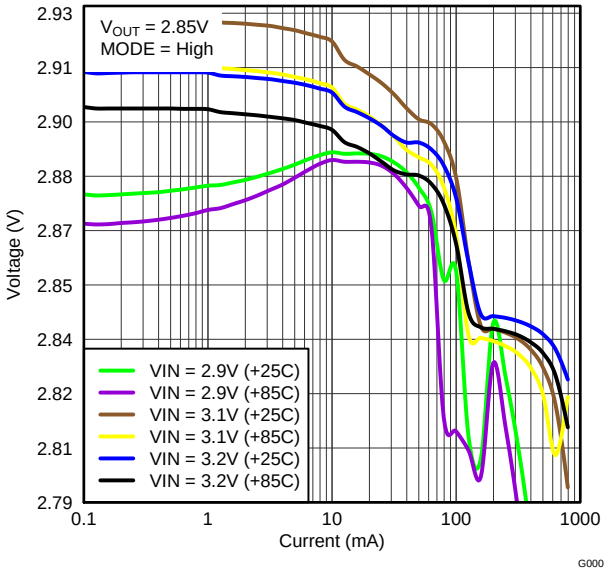


Figure 24.

DC OUTPUT VOLTAGE vs LOAD CURRENT

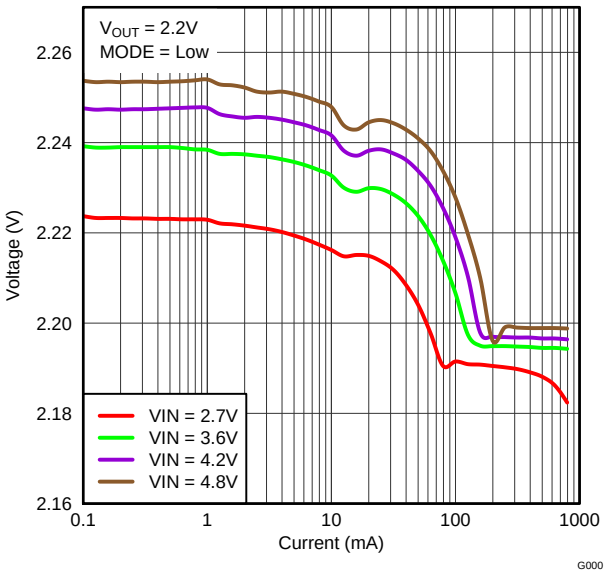


Figure 25.

PFM/PWM BOUNDARIES

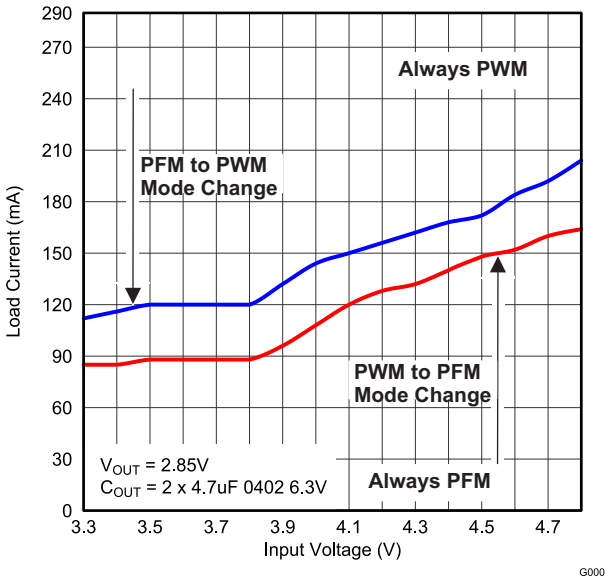


Figure 26.

TYPICAL CHARACTERISTICS (continued)

QUIESCENT CURRENT vs INPUT VOLTAGE

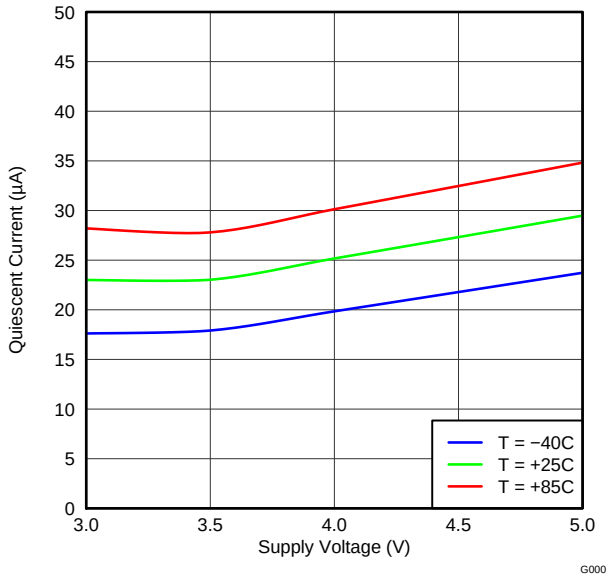


Figure 27.

PWM SWITCHING FREQUENCY vs INPUT VOLTAGE

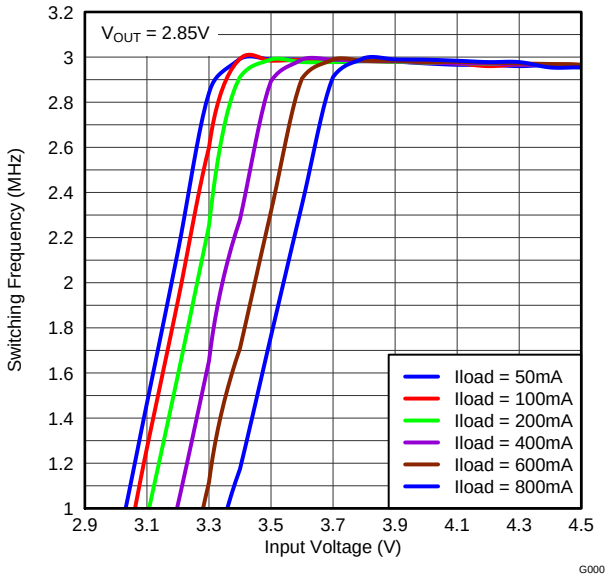


Figure 28.

PFM SWITCHING FREQUENCY vs INPUT VOLTAGE

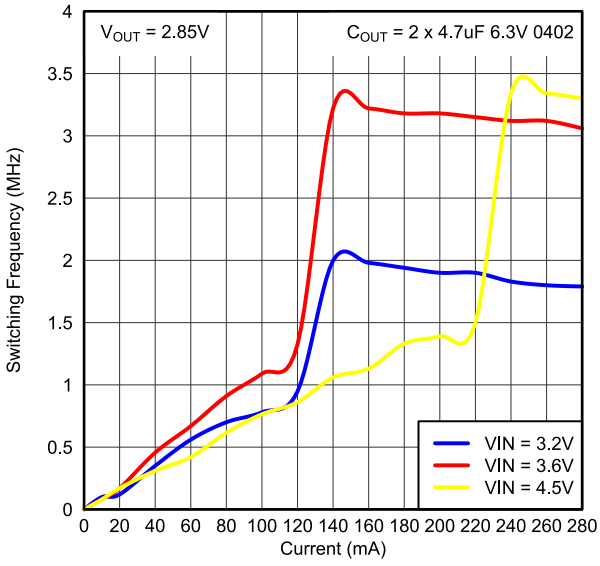


Figure 29.

P-CHANNEL $r_{DS(ON)}$ vs INPUT VOLTAGE

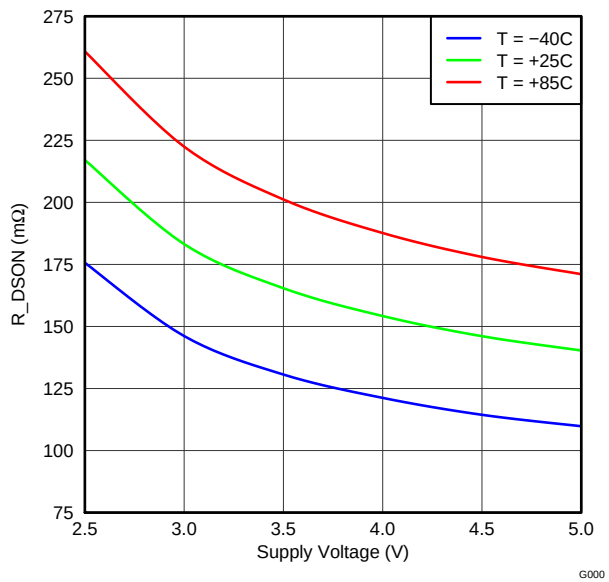


Figure 30.

TYPICAL CHARACTERISTICS (continued)

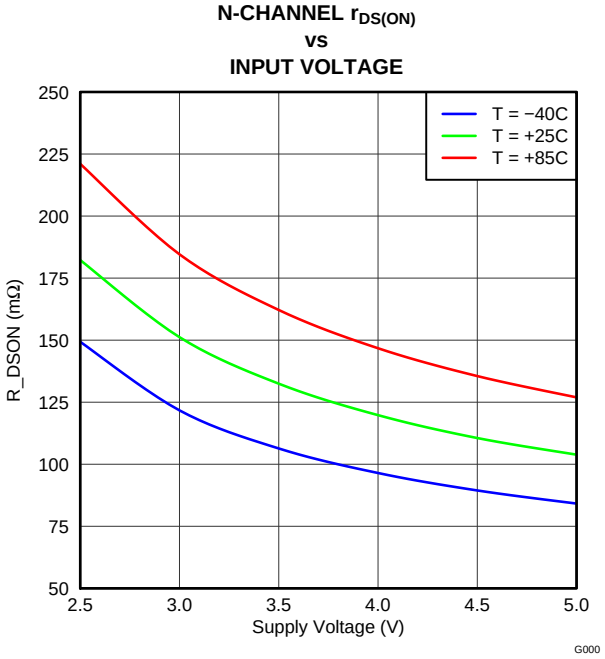


Figure 31.

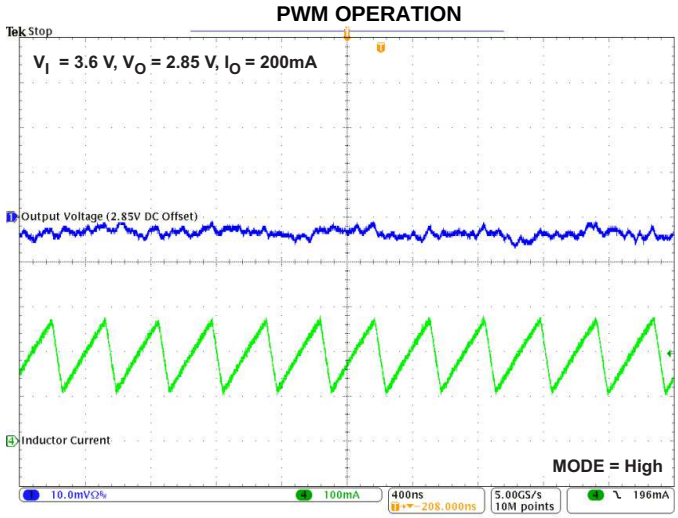


Figure 32.

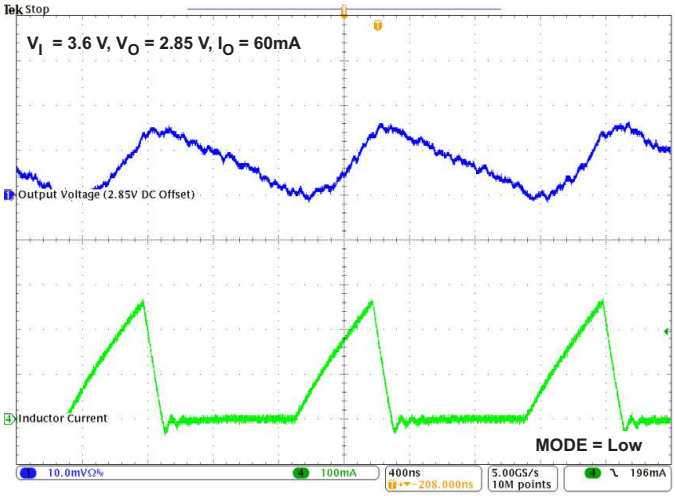


Figure 33.

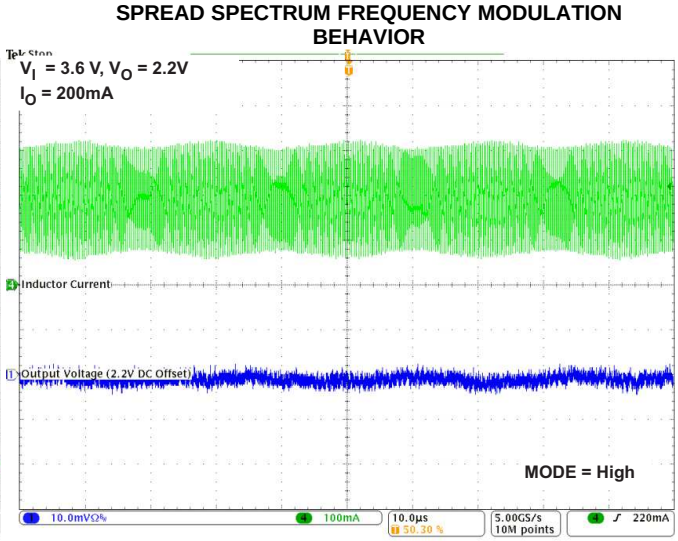


Figure 34.

TYPICAL CHARACTERISTICS (continued)

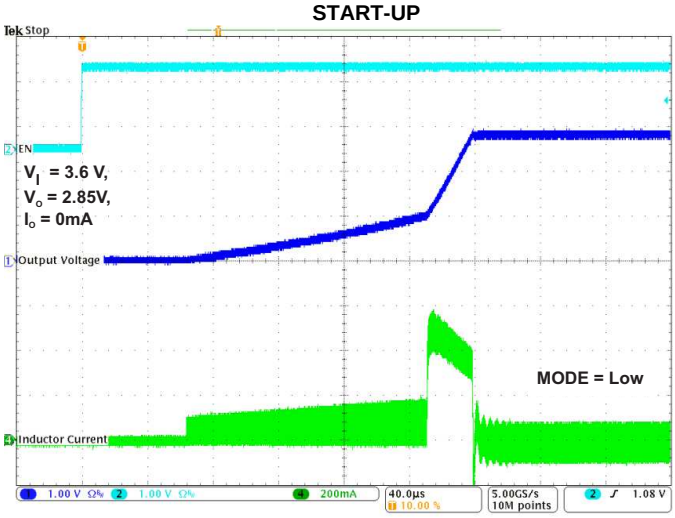


Figure 35.

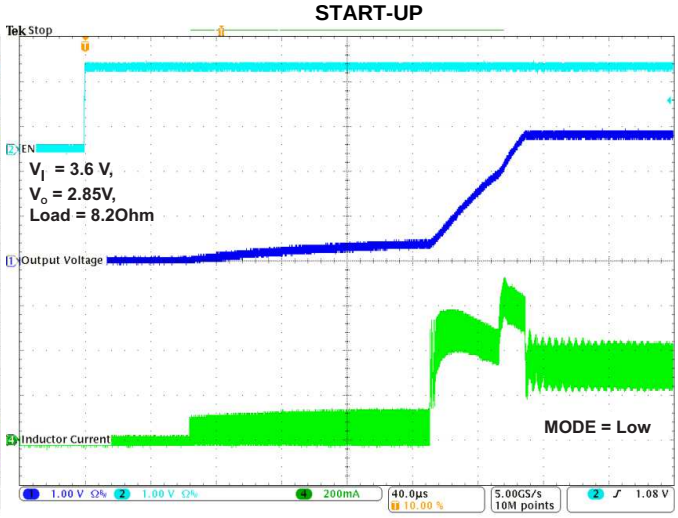


Figure 36.

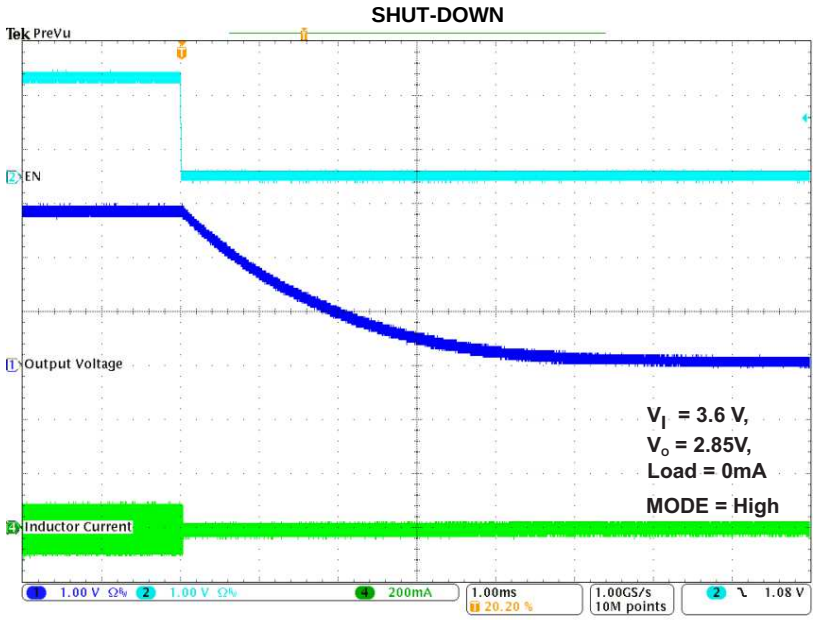


Figure 37.

DETAILED DESCRIPTION

OPERATION

The TPS62692 is a synchronous step-down converter typically operates at a regulated 3-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS62692 converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS62692 is inherently stable over a range of L and C_O.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 23 µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

SWITCHING FREQUENCY

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 5MHz to 7MHz, which is controlled to circa. 3 MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 3 MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 3 MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

POWER-SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically. During power-save mode the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFM on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

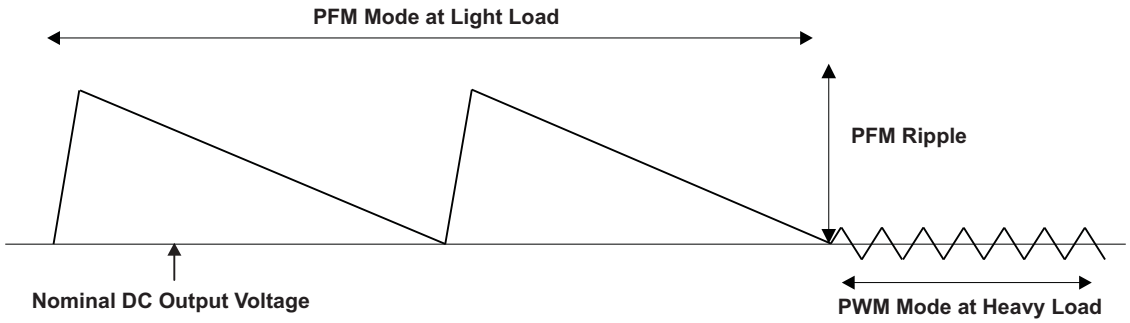


Figure 38. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique allowing simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

SPREAD SPECTRUM, PWM FREQUENCY DITHERING

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by ca. ±10% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

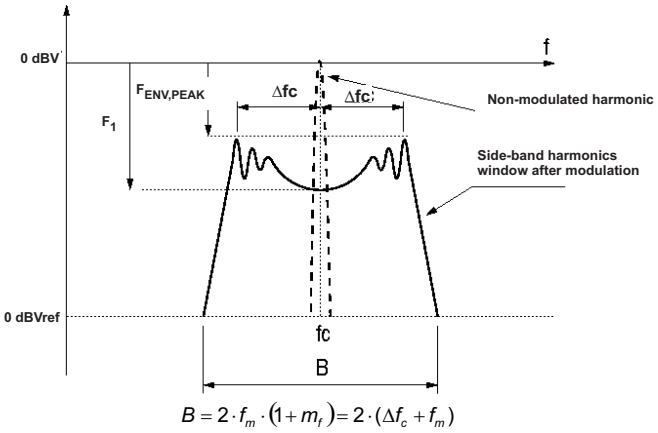


Figure 39. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time

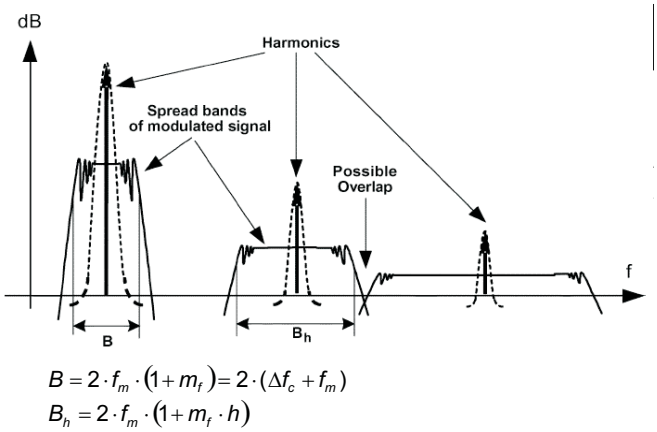


Figure 40. Spread Bands of Harmonics in Modulated Square Signals (1)

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

With:

f_c is the carrier frequency

f_m is the modulating frequency (approx. 0.008*f_c)

δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency f_c is limited by the process and finally the parameter modulation ratio (δ), together with f_m , which is the side-band harmonics bandwidth around the carrier frequency f_c . The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

f_m < RBW: The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

LOW DROPOUT, 100% DUTY CYCLE OPERATION

The device starts to enter 100% duty cycle mode once input and output voltage come close together. In order to maintain the output voltage, the P-channel MOSFET is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side switch is constantly turned on, thereby providing a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L) \tag{4}$$

(1) Spectrum illustrations and formulae (Figure 39 and Figure 40) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005. See REFERENCES Section for full citation.

With:

I_{OUT}max = Maximum output current, plus inductor ripple current.
$R_{DS(on)}$max = Maximum P-channel MOSFET $R_{DS(on)}$.
R_L = Inductor DC resistance.
V_{OUT}max = Nominal output voltage, plus maximum output voltage tolerance.

ENABLE

The TPS62692 device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.2 µA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

The TPS62692 device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 100 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value.

SOFT START

The TPS62692 has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

In the TPS62692, the soft start is implemented as a digital circuit increasing the switch current in steps of typically 300 mA, 700 mA, 1000 mA, and the typical switch current limit of 1250 mA. During the first phase the soft-start system progressively increases the on-time from a minimum pulse-width of 35 ns as a function of the output voltage, resulting in an current limit of approximately 300mA in this phase. The current limit transitions to the next step every 256 clocks (≈ 88us). To be able to switch from 700 mA to 1000 mA current limit step, the output voltage needs to be higher than 0.6 V (otherwise the parts keeps operating at 700 mA current limit).

After the soft-start time has exceeded and the output voltage settled at its nominal value, the converter supports the full load curent.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS62692 device has an UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.1 V input voltage.

SHORT-CIRCUIT PROTECTION

The TPS62692 integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4 V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5 V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

APPLICATION INFORMATION

INDUCTOR SELECTION

The TPS62692 series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.5µH to 1.8µH and with output capacitors in the range of 4.7 µF to 10 µF. The internal compensation is optimized to operate with an output filter of L = 1 µH and C_O = 4.7 µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

with: f_{SW} = switching frequency (4 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current (5)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance $_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6269x converters.

Table 1. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS (in mm)
MURATA	LQM21PN1R0NGC	2.0 x 1.2 x 1.0 max. height
	LQM21PN1R5MC0	2.0 x 1.2 x 0.55 max. height
FDK	MIPS2012D1R0-X2	2.0 x 1.2 x 1.0 max. height
TAIYO YUDEN	NM2012N1R0M	2.0 x 1.2 x 1.0 max. height
TOKO	MDT2012-CH1R0A	2.0 x 1.2 x 1.0 max. height
	MDT2012-CR1R0	2.0 x 1.2 x 1.0 max. height

OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS62692 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 2µF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 4.7 µF or 10 µF ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is ca. 0.5% to 1.5% of the nominal output voltage V_O.

The output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger once. Increasing the output capacitor value and the effective inductance will minimize the output ripple voltage.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2 or 4.7-µF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy should be found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6269x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The ground pins of the dc/dc converter must be strongly connected to the PCB ground (i.e. reference potential across the system). These ground pins serve as the return path for both the control circuitry and the synchronous rectifier. Furthermore, due to its high frequency switching circuitry, it is imperative for the input capacitor to be as close to the SMPS device as possible, and that there is an unbroken ground plane under the TPS6269x and its external passives. Additionally, minimizing the area between the SW pin trace and inductor will limit high frequency radiated energy. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

The output capacitor carries the inductor ripple current. While not as critical as the input capacitor, an unbroken ground connection from this capacitor's ground return to the inductor, input capacitor and SMPS device will reduce the output voltage ripple and it's associated ESL step. This is a critical aspect to achieve best loop and frequency stability.

High frequency currents tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias in the surrounding of the dc/dc converter leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PCB (i.e. onto which the components are located).

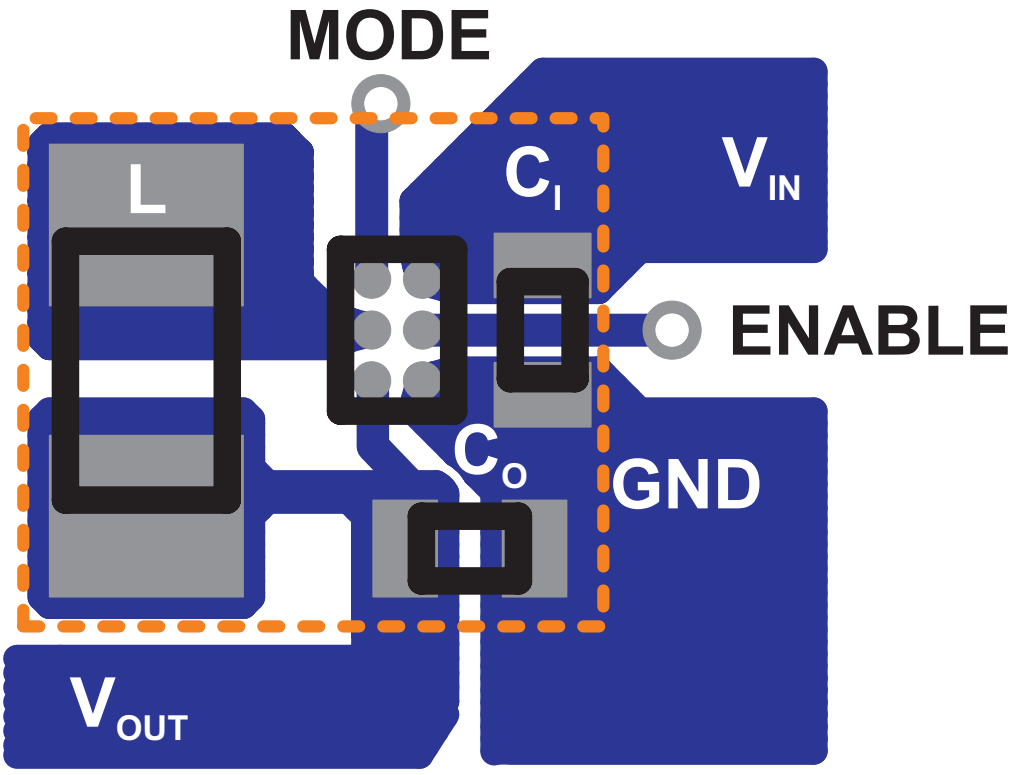


Figure 41. Suggested Layout (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS62692 devices is 105°C. The thermal resistance of the 6-pin CSP package (YFD-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW.

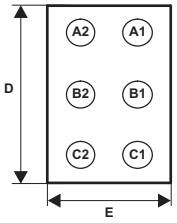
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{125°C/W} = 160mW \quad (6)$$

REFERENCES

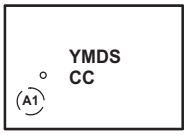
"EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques", in *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 4, NO. 3, AUGUST 2005, pp 569-576* by Josep Balcells, Alfonso Santolaria, Antonio Orlandi, David González, Javier Gago.

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Code:

- YM — Year Month date Code
- D — Day of laser mark
- S — Assembly site code
- CC— Chip code

CHIP SCALE PACKAGE DIMENSIONS

The TPS62692 device is available in an 6-bump chip scale package (YFD, NanoFree™). The package dimensions are given as:

D	E
Max = 1.33 mm	Max = 0.956 mm
Min = 1.27 mm	Min = 0.896 mm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62693YFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UD	Samples
TPS62693YFDT	ACTIVE	DSBGA	YFD	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UD	Samples
TPS62698YFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7	Samples
TPS62698YFDT	ACTIVE	DSBGA	YFD	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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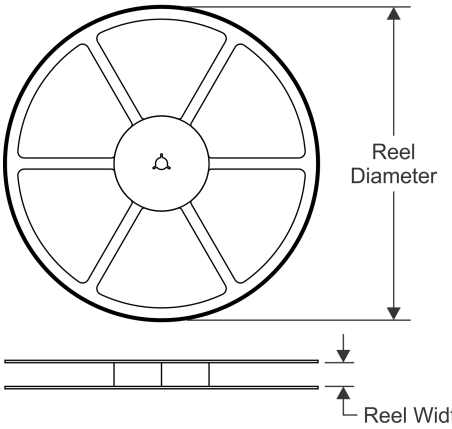
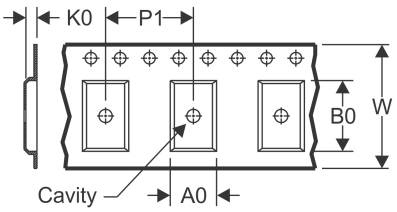
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

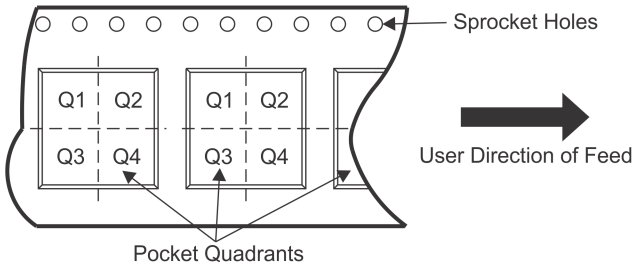


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

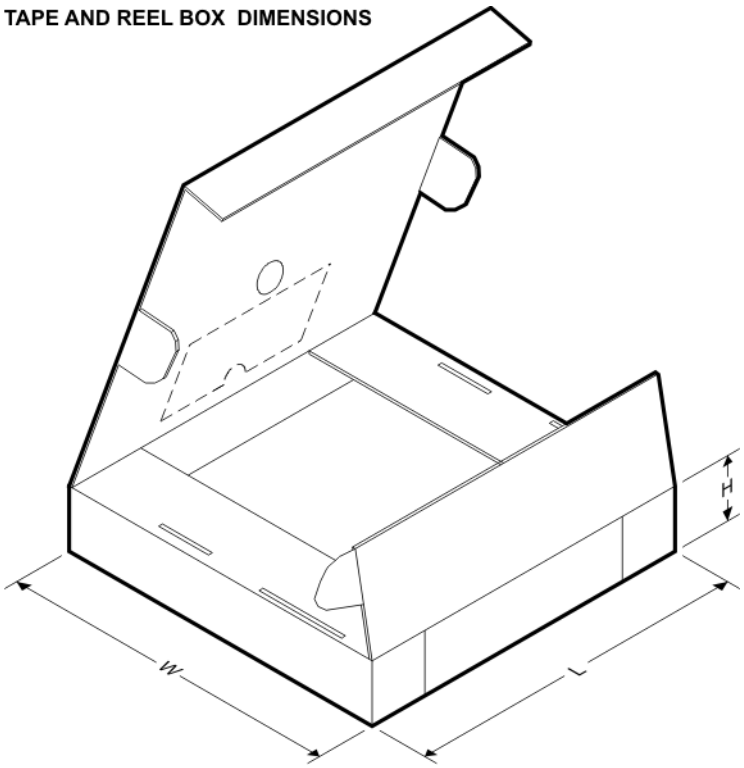
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62693YFDR	DSBGA	YFD	6	3000	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62693YFDT	DSBGA	YFD	6	250	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62698YFDR	DSBGA	YFD	6	3000	180.0	8.4	1.03	1.53	0.56	2.0	8.0	Q1
TPS62698YFDT	DSBGA	YFD	6	250	180.0	8.4	1.03	1.53	0.56	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

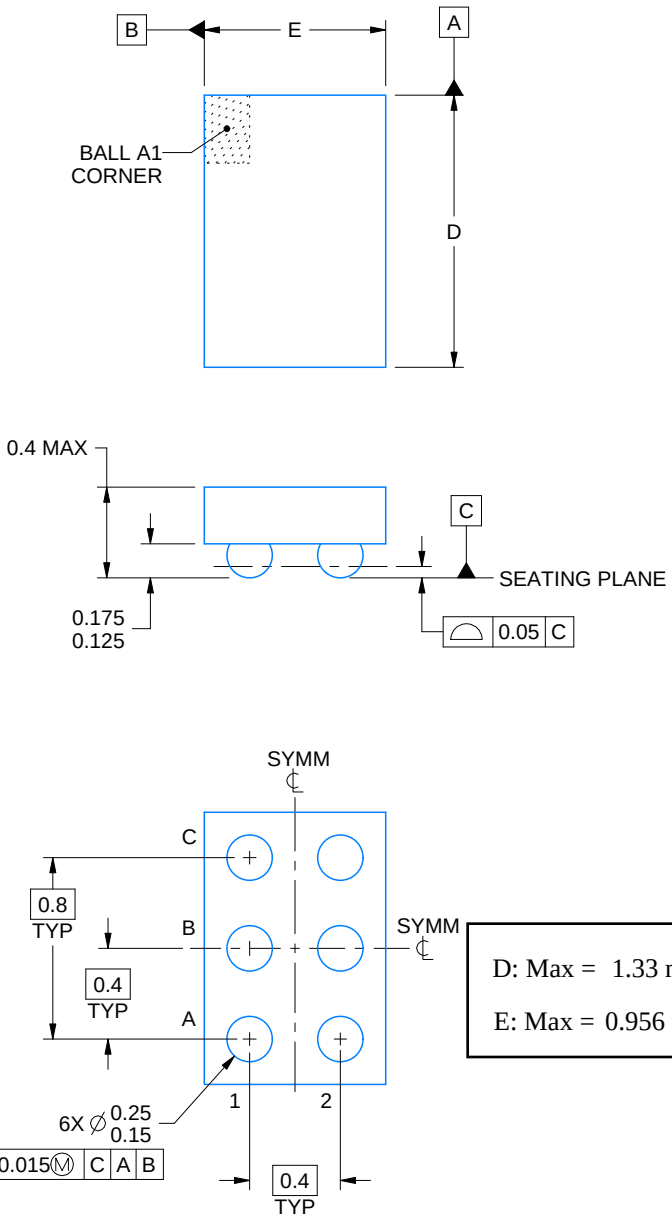
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62693YFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
TPS62693YFDT	DSBGA	YFD	6	250	210.0	185.0	35.0
TPS62698YFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
TPS62698YFDT	DSBGA	YFD	6	250	182.0	182.0	20.0

YFD0006

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.33 mm, Min = 1.27 mm

E: Max = 0.956 mm, Min =0.896 mm

4219510/A 11/2019

NOTES:

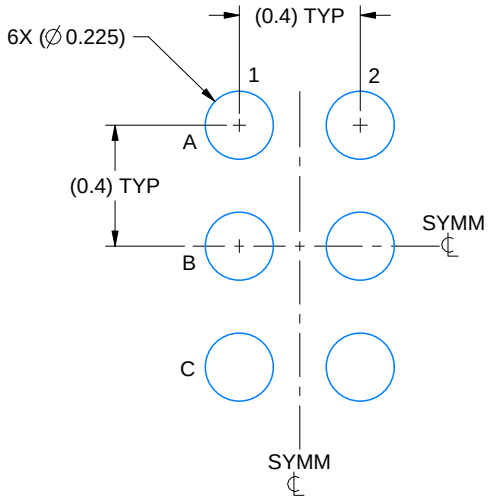
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

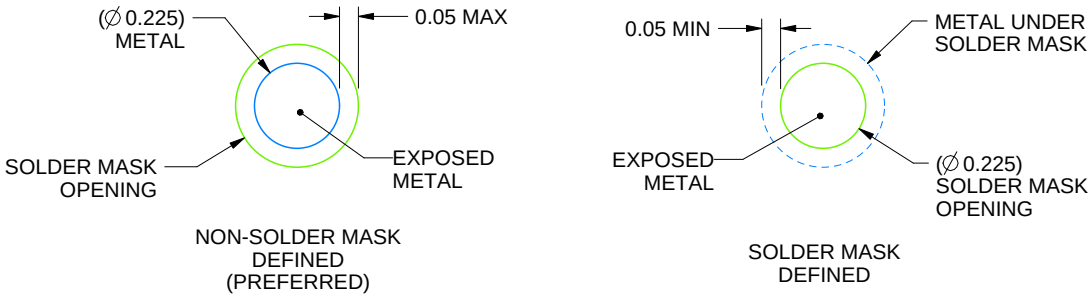
YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

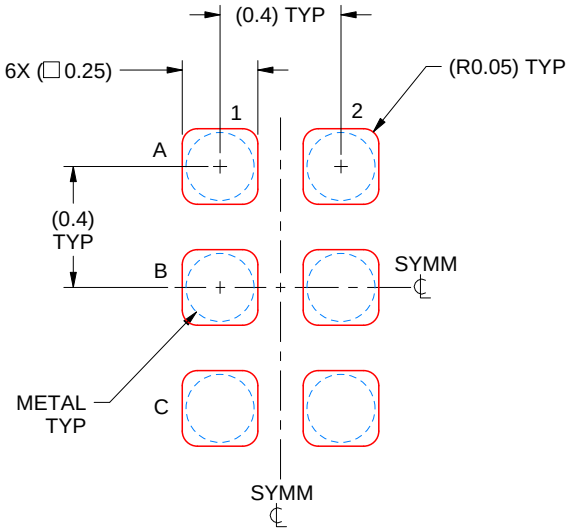
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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